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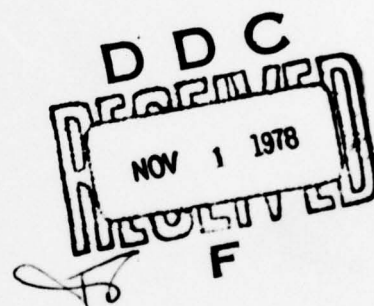
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CORADCOM-77-0190-3

VEHICULAR INTERCOMMUNICATION SYSTEM

C. F. Wedaman
CINCINNATI ELECTRONICS CORPORATION
2630 Glendale-Milford Road
Cincinnati OH 45241



October 1978

Third Quarterly Report for Period 1 April - 31 July 1978

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Prepared for:
Project Manager SINCGARS
ATTN: DRCPM-GARS-LM
Fort Monmouth NJ 07703

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
18 CORADCOM 77-0190-3		9
4. TITLE (and Subtitle)	5. TYPE OF REPORT & PERIOD COVERED	
6 Vehicular Intercommunication System.	Quarterly Report. no. 3, 1 Apr 1978-31 Jul 1978.	
7. AUTHOR(s)	8. CONTRACT OR GRANT NUMBER(s)	
10 C. F. Wedaman	15 DAAB07-77-C-0190	
9. PERFORMING ORGANIZATION NAME AND ADDRESS	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS	
Cincinnati Electronics Corporation 2630 Glendale-Milford Road Cincinnati OH 45241	694365.437.80.03.01	
11. CONTROLLING OFFICE NAME AND ADDRESS	12. REPORT DATE	
Project Manager, SINCGARS ATTN: DRCPM-GARS-LM Ft. Monmouth NJ 07703	11 Oct 1978	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	13. NUMBER OF PAGES	
Commander US Army Communications Research & Development Command ATTN: DRDCO-COM-RN-3 Ft. Monmouth NJ 07703	52	
16. DISTRIBUTION STATEMENT (of this Report)	15. SECURITY CLASS. (of this report)	
Approved for Public Release, Distribution Unlimited.	Unclassified	
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
12 56p		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
Vehicular Intercom, Wireless Intercom, Voice Signal Multiplexing, Inductive Radiators, Infrared and Microwave Pulsed Transceivers, Batteries		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)		
This is the third quarterly report for the design study of a vehicular intercommunication system primarily used in tracked vehicles. The report covers the time period from 1 April through 31 July 1978. Accomplishments for the period include bread-board studies of multiplex systems for signal routing and analysis of inductive, infrared, and microwave wireless transmission systems, and batteries.		

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SECTION I

INTRODUCTION

This is the Third Vehicular Intercom System Study Quarterly Report and covers technical progress from 1 April 1978 to 31 July 1978. This report covers four months which reflects an approved 30-day extension of contract delivery item due dates.

SECTION II

CONTRACT DELIVERY SCHEDULE

CLIN	1977				1978											
	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	
0002 Technical Data Exhibit A																
A001 Quarterly Reports				#1 D Δ G Δ	F Δ	D Δ G Δ	#2 D Δ G Δ	F Δ			#3 D Δ G Δ	F Δ				
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- Plan																
A004 LSA Model																
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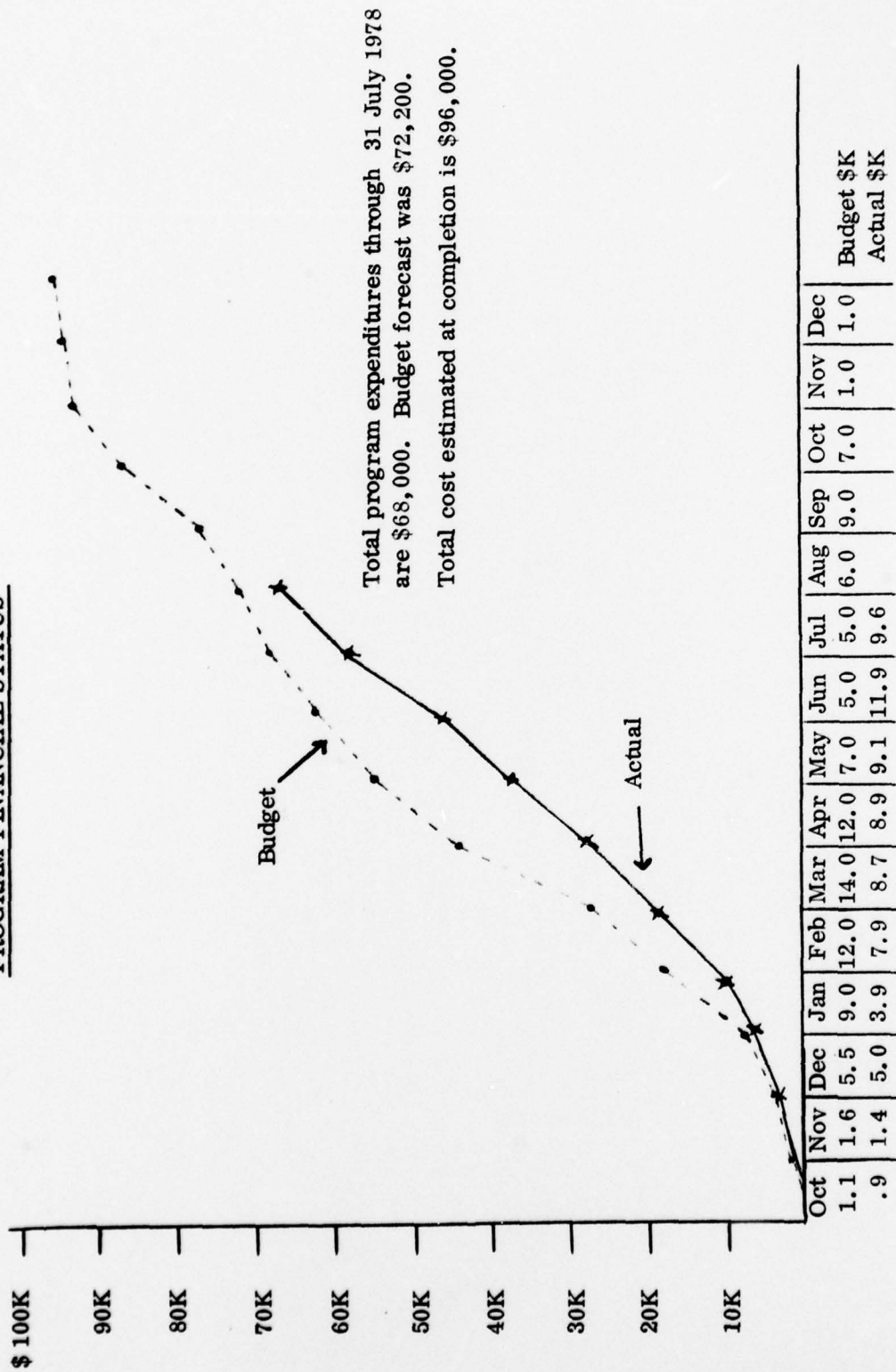
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* = Actual

NOTE: Schedule reflects approved 30-day extension of delivery items. The 30-day extension was requested in July 1978.

SECTION III

PROGRAM FINANCIAL STATUS



SECTION IV

RESULTS OF STUDIES

A. GENERAL

Two basic techniques have been considered for multiplexing information in order to reduce or eliminate the intercom system wiring. They are: Frequency Division Multiplexing (FDM) and Time Division Multiplexing (TDM). In general, the FDM system uses simpler electronics and requires a linear wideband transmission system, while the TDM system uses more complex electronics and can use a pulsed transmission system due to the digital nature of the data to be transmitted. At this point in the study effort, no conclusion has been drawn as to which system is best. This decision will be made after all systems have been studied; cost versus performance trade-offs have been compiled; and these discussed with potential users of the system. This report presents results of current studies of the FDM and TDM systems and wireless techniques.

B. MULTIPLEX SYSTEMS

1. Frequency Division Multiplexing

a. Technical Feasibility

Cincinnati Electronics proposed a Frequency Division Multiplexing intercom comprised of monitor audio and microphone audio systems. The monitor audio system reduced cable size by frequency multiplexing the intercom and receiver audios using voltage control oscillators. These audio signals were cabled by one wire to the crew control box and recovered using a phase-lock loop. The microphone audio system reduced cable size by putting DC control voltages on the same wire that the microphone audio was on. The DC control voltage was monitored at the main junction box and used to route the microphone audio to the proper transmitter or to intercom circuits. In previous reports, both microphone and monitor audio systems have been analyzed to discover potential problems with the FDM approach from a technical viewpoint. The most difficult to analyze system was the monitor audio approach. VCO's and PLL's were chosen based on temperature drift, cost, and availability of vendors. Once chosen, devices were ordered and a breadboard was built. This breadboard revealed a distortion problem caused by phase detector products; simple bandpass filters solved this problem. Hence, neither the phase detector problem nor other problems have been found which cannot be readily resolved during the final system design. As a consequence, the Cincinnati Electronics proposed Frequency Division Multiplexing scheme is considered technically feasible as a means of reducing cable size and number of wires.

b. FDM Compared to TDMA

To achieve Time Division Multiplexing of audio signals, these signals have to be converted into a digital pattern. Also, to control inputting and extraction of information, considerable control logic and accurate clocks are required. These circuits are not required in the Cincinnati Electronics FDM system; and, as a consequence, the overall circuitry is considerably simpler. Cincinnati Electronics Logistic Support Analysis Modeling (LSAM) Report, dated May 1978, shows that for a completely wired intercom system like the existing VIC, the FDM approach is less expensive, more reliable and easier to maintain. However, a completely wired system would not meet the wireless audio accessory requirement for VIS.

To achieve the wireless requirement for the FDM system, Cincinnati Electronics proposed an inductive radiator system using VLF frequencies. Sufficient bandwidth is not available at these frequencies to use the inductive approach for TDMA. However, a wireless FDM system will still have a crew control box and cables to the intercom junction box because of the proposed microphone audio multiplexing scheme. On the other hand, TDMA which outputs a digital stream can pulse modulate microwave or infrared transmitters which would flood the vehicle with data. These pulses could be detected anywhere within the vehicle; and, hence, a crew control box and cabling to this box would not be required. This reduction in cabling and boxes could offset the cost advantage of the simpler Cincinnati Electronics FDM system. Therefore, which multiplexing system is best depends heavily on the feasibility of wireless and the proposed means of achieving wireless.

2. Minimum Wire Time Division Multiplexing

a. Introduction

The TDMA technique and design approach discussed in the previous quarterly reports has been breadboarded and several problems have been discovered. The frame organization as originally conceived (see Figure 4-1) imposes some timing constraints which make the overall system difficult to implement. The control station design is relatively straightforward with some relatively minor problem areas. The user station design concept of using variable length shift registers and maintaining a constant shift length equal to the frame length makes it necessary to use separate input and output data lines to each of the user stations. This design defeats the intent to use a single data loop around the vehicle for a minimum wire system.

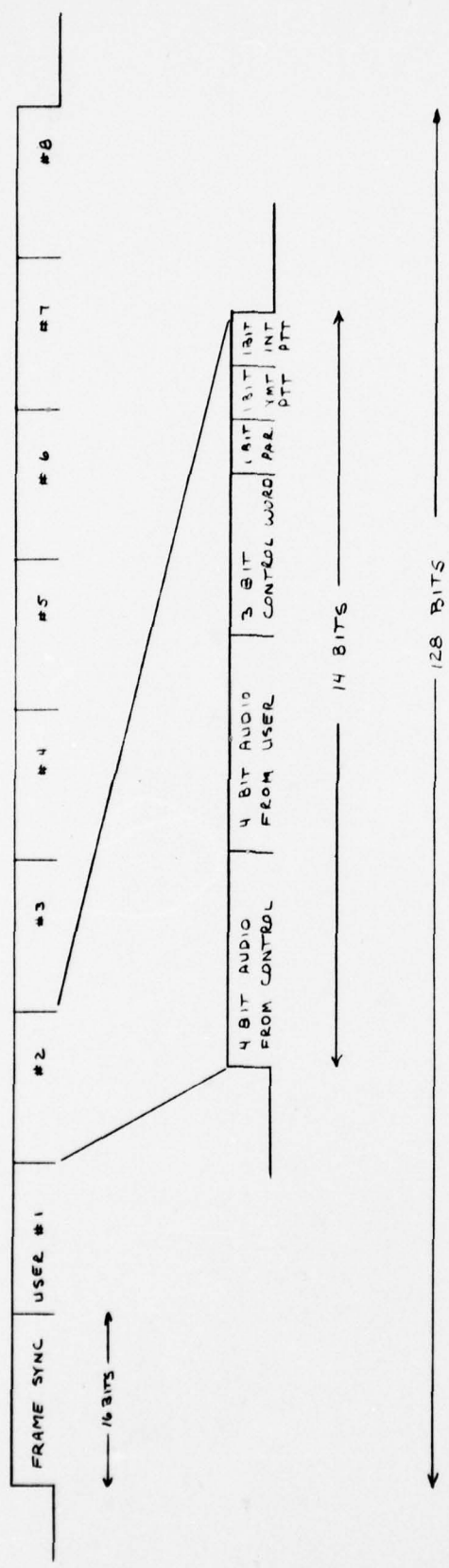


FIGURE 4-1. ORIGINAL FRAME STRUCTURE

b. Frame Reorganization

In order to resolve these problems, a new frame organization and system design has been implemented. The new frame organization is shown in Figure 4-2. The overall frame length is the same as before but a more conventional approach has been used in its structure. Each subscriber is assigned an unique time slot in the frame. A subscriber is defined as an audio source, so each user as well as each of the three RT's, the intercom and "ALL" is assigned an unique time slot. Each of the eight user slots is identical in format and is eleven bits long. The first four bits are digitized audio from the user, the next three bits (four including parity) make up the destination address which tells the controller which of the RT's, intercom or ALL the user has selected. The next two bits are transmit PTT and intercom PTT respectively. The eleventh bit is a guard bit to separate time slots.

The remaining five subscriber slots are assigned to the three RT's, the intercom and ALL. These slots are organized with four bits of digitized audio and one guard bit.

In actual operation, the user would select RT #1 for example. The destination code for RT #1 would be inserted in the proper position of the user's time slot and the user station would select RT #1's time slot as its CVSD input.

c. Control Station Block Diagram

A block diagram of the revised VIS Controller is shown in Figure 4-3. The function of each of these blocks will be briefly described here.

- 1) Master Clock - This circuit generates all high speed (1 MHz) data clocks as well as the low speed (32 kHz) clocks for audio processing in the CVSD's.
- 2) Synchronization and Input Data - A fifteen-bit sync pattern is generated and inserted onto the data stream at the beginning of each frame. This same circuit also provides user data in parallel form.
- 3) Output Enable Control - During those periods of time when the Controller is not putting data on the data line, this circuit causes a high impedance to be presented to the data line to prevent distortion of user data.
- 4) Input Data Control and Steering - The controls necessary to load and steer data from each of the eight users to their proper destination are generated in this section.

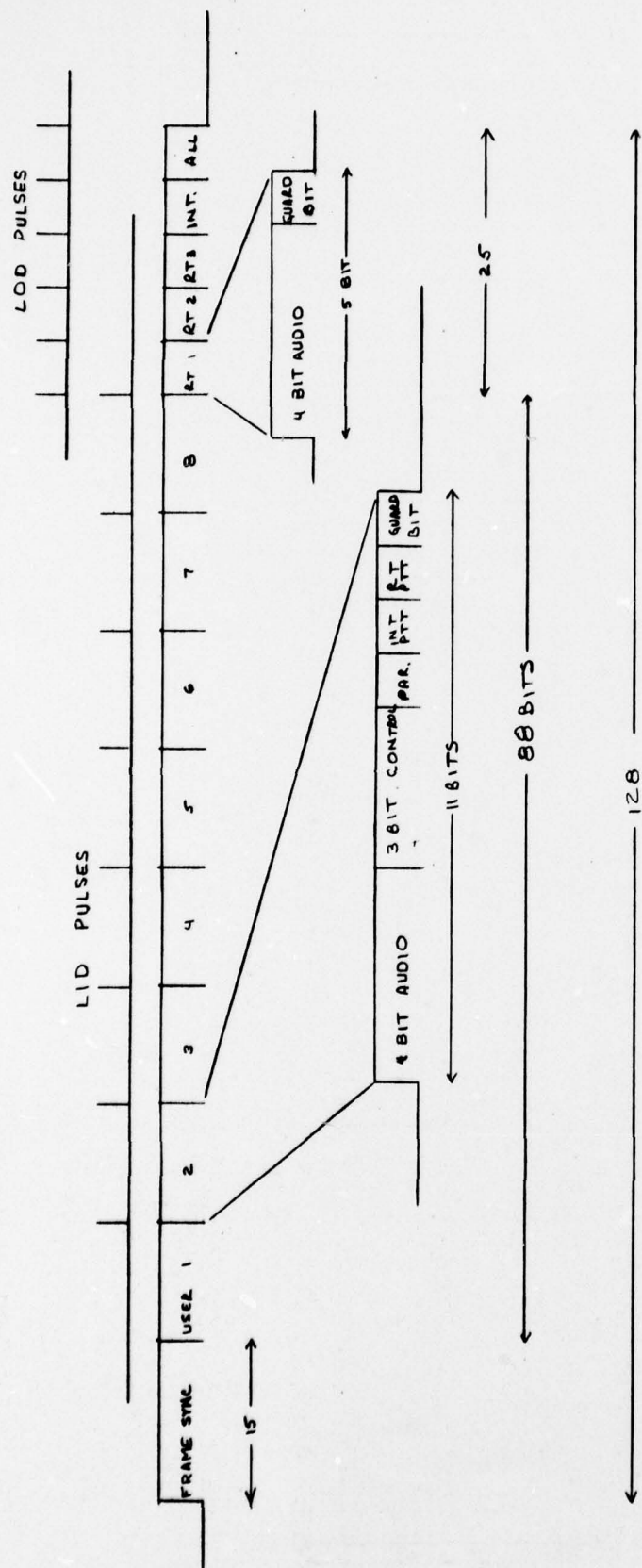
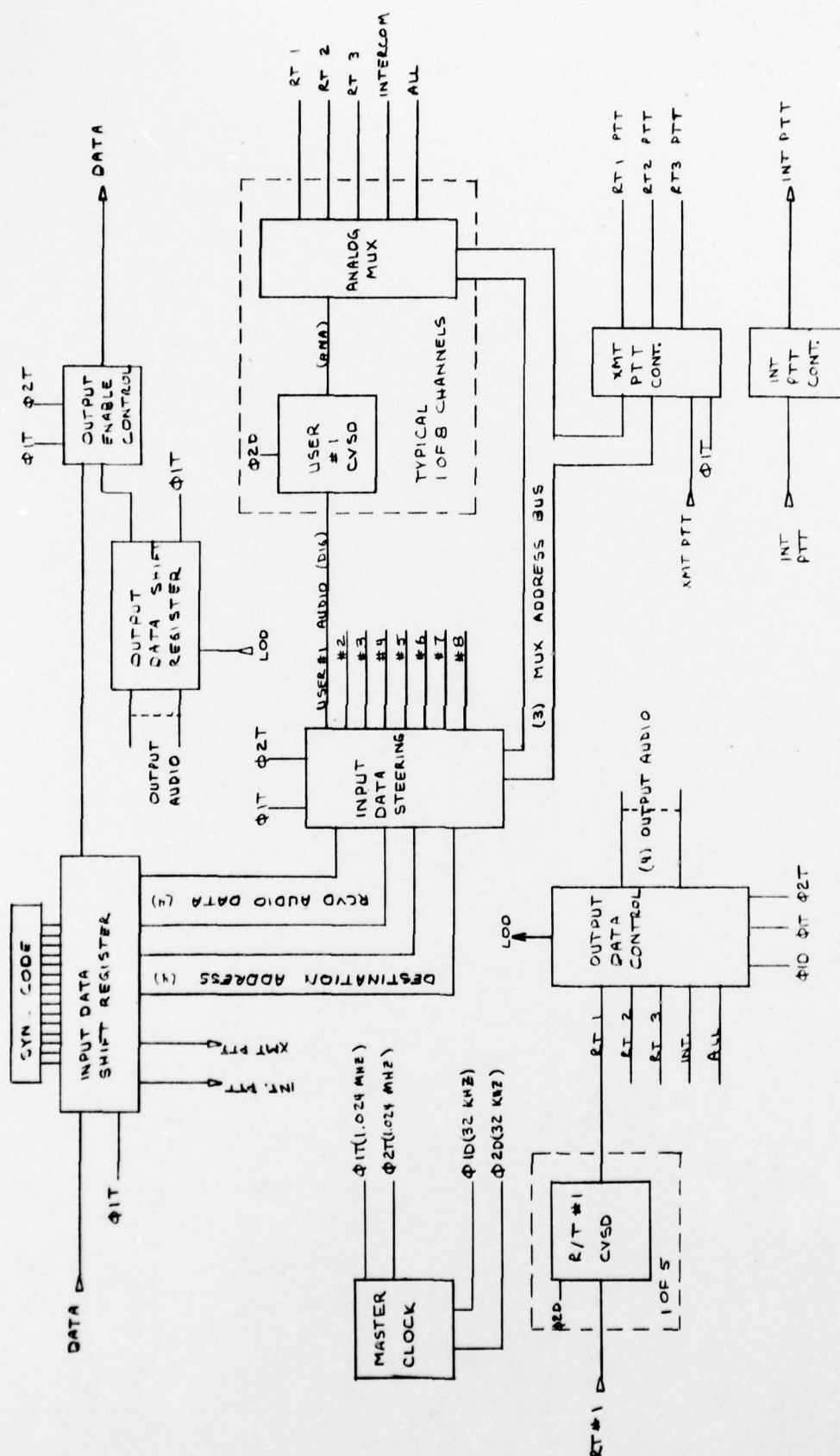


FIGURE 4-2. REVISED FRAME STRUCTURE



5) Output Data Control and Steering - Loading and steering control circuitry in this section insures that the proper audio is loaded into each of the last five time slots in the frame. The output data shift register receives output audio data in parallel block form and inserts it into the data stream in serial form at the proper time.

6) Transmit PTT - Each user's transmit PTT bit is steered by this circuit to the selected RT.

7) Intercom PTT - This circuit recognizes a PTT from only one of the eight users to provide a lockout function for the remaining PTT lines.

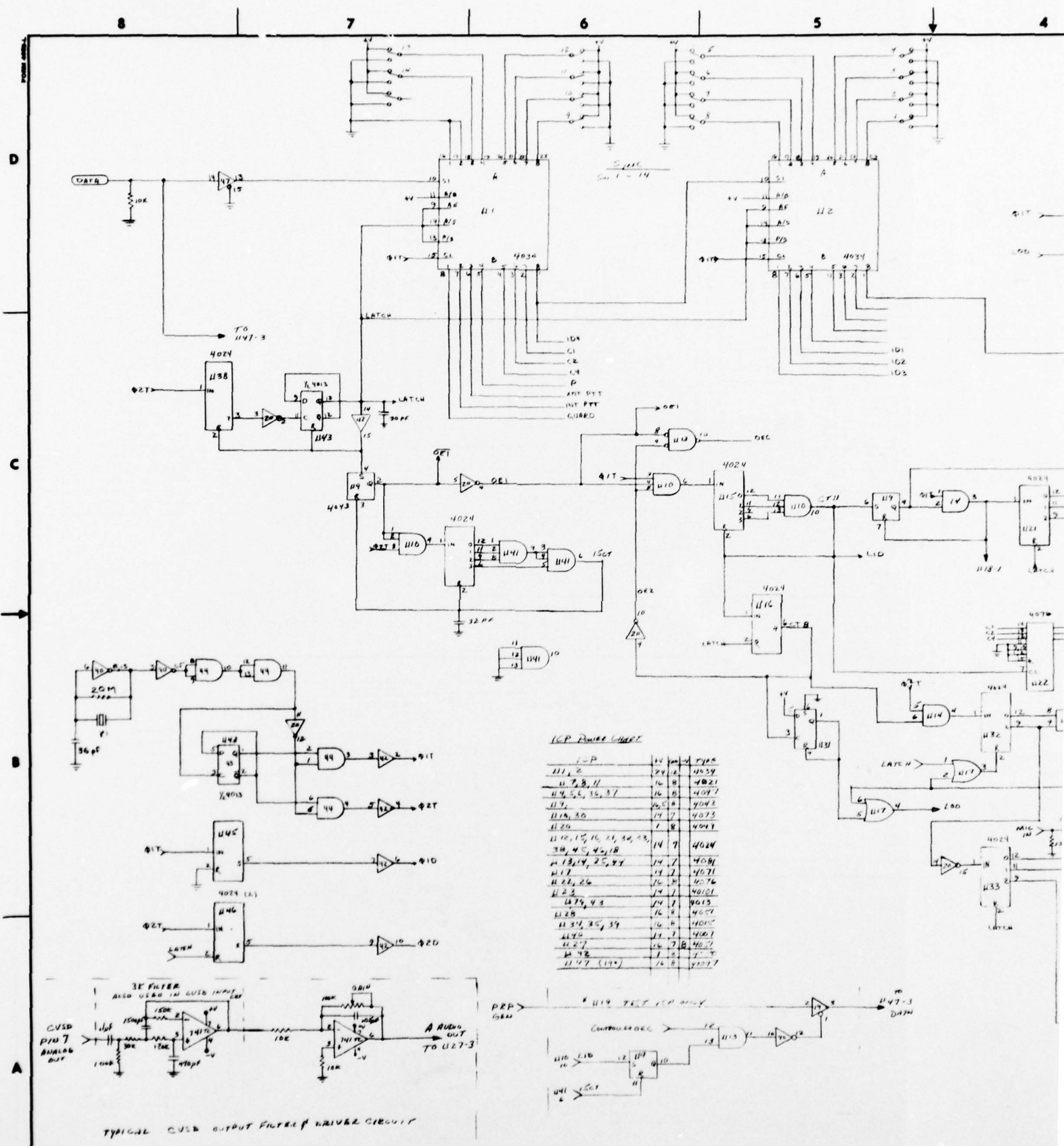
d. Control Station Schematic

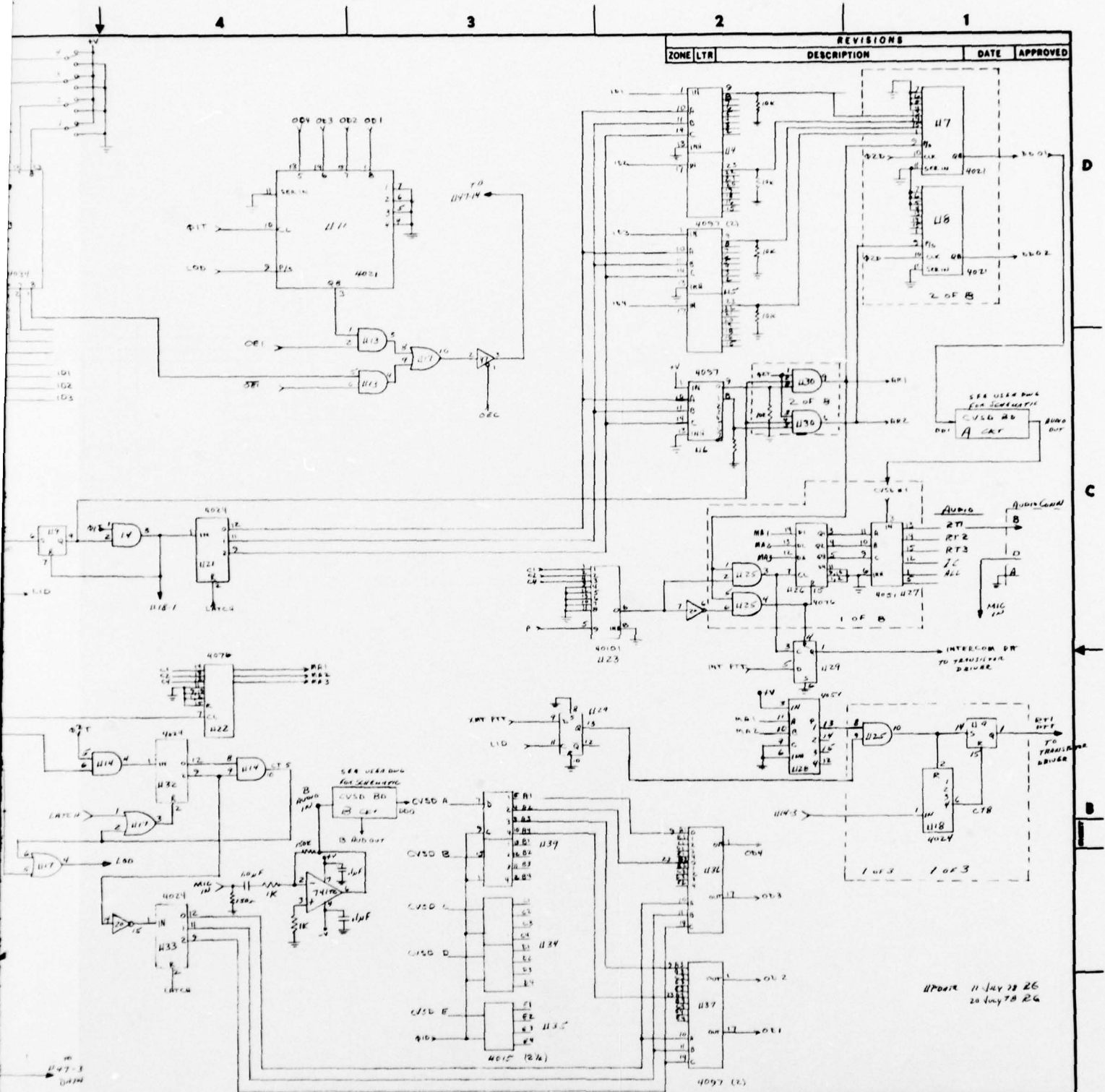
Figure 4-4 is a schematic diagram of the revised VIS controller as breadboarded. Each of the functional blocks described above will be discussed in detail.

1) Master Clock - U40 and Y1 make up the VIS master clock operating at 2.048 MHz. The oscillator is followed by three stages of buffering and waveshaping to create a square wave. The 2.048 MHz clock is then divided by 2 by U43 and then gated by two sections of U44 to create a two-phase nonoverlapping clock with each phase at 1.024 MHz. U45 and U46 divide the 1.024 MHz data clock down to 32 kHz to clock the CVSD's and the slow speed shift registers. Both phases of the data clock and both phases of the slow speed clock are then buffered by four sections of U42.

2) Synchronization and Input Data - Counter U38 and U43 determine the beginning of frame and the frame length. Every 128 \emptyset 2 clocks a pulse is generated called Latch. Latch initializes all circuits in the controller to their start of frame condition and loads the fifteen-bit sync pattern into the "A" ports of shift registers U1 and U2. The sync pattern is determined by the position of the 15 switches. When the sync pattern has been shifted out of U1 and U2, these same devices serve as data input shift registers with user data available in parallel form at the "B" ports.

3) Output Enable Control - The controller data output must be enabled for the 15-bit period of the sync pattern and the final 25 bits of the frame. Counter U12 is enabled by Latch and counts 15 \emptyset 2 clocks and stops. Flip-flop U9 is set by Latch and reset by count 15 to create the output enable pulse for the sync period. Counter U16's output is used as the enable control for the final 25 bits since its output goes high at count 103 and is reset by Latch at count 128.





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NEXT ASSY USED ON		DRAWN <i>R. L. Jones</i> DATE 5-25-78		FIGURE 4-4. VIS CONTROLLER, REVISION 1	
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4) Input Data Control and Steering - Counter U15 is enabled after the sync pattern has been transmitted (count 15) and generates a Latch Input Data (LID) pulse every eleven ϕ_1 clock pulses. The LID pulses are counted by U16 and the eighth pulse is used to disable further generation of LID pulses until the next frame. The LID pulses are positioned in time as shown in Figure 4-2 such that the user data appears at the "B" ports of U1 and U2 in their proper location. Each LID pulse is stretched to one full clock period by U9 and U14 to be used in generating a parallel latch pulse to one of eight parallel-to-serial converter shift registers. A delayed LID pulse is available at the output of U14 which is used to clock station counter U21.

U4 and U5 are digital data multiplexers and along with station counter U21 form the input audio steering circuitry. The station counter's three-bit binary output is set to zero with Latch at the beginning of each frame. The counter is then incremented by the LID pulse delayed by $1/2$ period of ϕ_1 . These three bits are the address bits to the dual one of eight data multiplexers U4 and U5. The data inputs are the four bits of digitized audio from the user. Thus, the four bits of audio are steered through U4 and U5 to one of eight four-bit shift registers, two of which are shown on the schematic as U7 and U8. The input latch pulses for these shift registers are generated from the stretched LID pulse, one of eight outputs from U6 and ϕ_2 clock. These shift registers are clocked at 32 kHz and receive new input data every 125 μ s to create a continuous data stream which is fed directly to a CVSD for conversion to analog audio.

Destination address bits C1, C2, and C4 from the user are also latched by the LID pulses into U22 to create analog multiplexer address bits MA1, MA2, and MA3. U26, U27, and two sections of U25 show one of eight channels of analog audio steering circuitry, the circuit shown being used for user station number one. User number one's destination address is latched into U15 by the conditioned LID pulse discussed earlier gated by a correct parity bit. Parity is checked by U23 based on C1, C2, and C4 and compared to the transmitted parity bit. An incorrect parity bit would set the latched destination address to zero which is an unused condition. Analog multiplexer U27 then steers user number one's audio to the destination selected at the user station.

7) Intercom PTT - The intercom PTT bit from user station number 1 is the only one recognized by the Controller. This intercom PTT bit is latched into U29 and can be used as a control line to block other users PTT requests. Therefore, user number 1 could be designated as "Commander".

e. User Station Block Diagram

Figure 4-5 is a block diagram of the revised VIS User Station. Each of the sections will be briefly described here on a functional level. A more detailed discussion of the user station will follow.

- 1) Clock - The two-phase clock is received from the Controller and passed to the user circuitry. A low speed clock is also derived from Ø2T.
- 2) Data Shift Register - The serial data stream is directed through this register to be converted to parallel form. Transmit data is also loaded into this section.
- 3) Sync Recognition and Recovery - The serial data stream is examined in this section for the sync pattern in order to establish synchronization between the user and the Controller. This circuit also will detect missed sync patterns and provide for synchronization recovery.
- 4) Output Data and Loading - The ten bits of user generated data come from this section. Four bits of digitized audio, a three-bit destination address plus parity, transmit and intercom PTT. This circuit also generates the controls necessary to load the data into the serial data stream at the proper time.
- 5) Output Enable Control - The output control allows the data from the user to be put on the serial data stream only at the proper time. This is to prevent possible data distortion in the event of missed sync.
- 6) Input Data Selection and Loading - The operator can select one of five audio sources with the audio select switch. The information from this switch is used to select the proper time slot within the frame and load it into a shift register to be sent to the CVSD for decoding.
- 7) CVSD - The CVSD selectively encodes analog audio or decodes digital audio depending on the state of PTT.

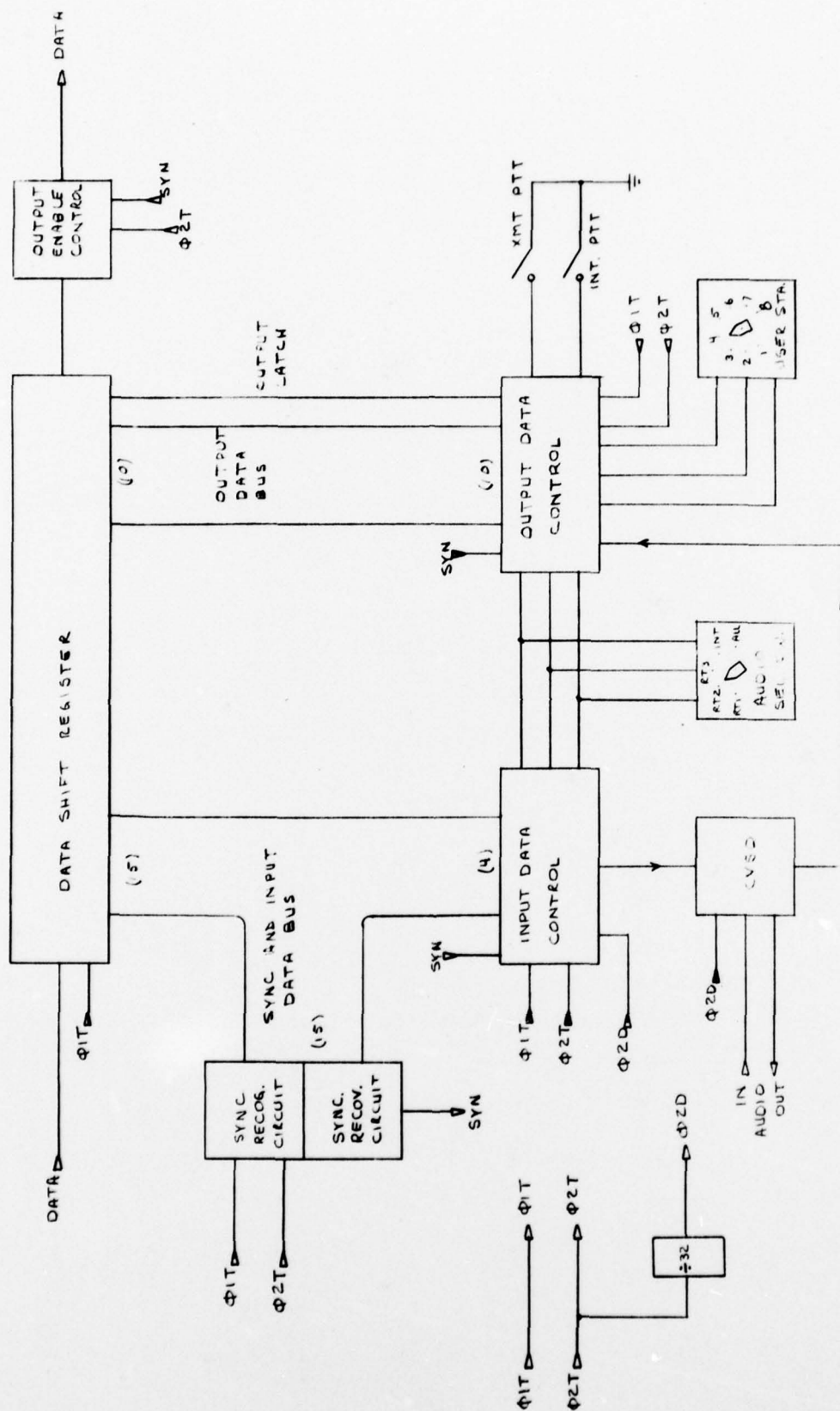


FIGURE 4-5. REVISED VIS USER STATION BLOCK DIAGRAM

5) Output Data Control and Steering - The output of counter U16 going high indicates that frame sync and the eight user station time slots have been transmitted. Flip-flop U31 uses this positive going edge to generate the first of five Latch Output Data (LOD) pulses. These pulses latch the four selected bits of digitized audio from multiplexers U36 and U37 into the output shift register U11. Counter U32 is also enabled with the output of counter U16 and is used to generate the remaining four LOD pulses every five $\phi 2$ clocks. The five LOD pulses are positioned in time as shown in Figure 4-2.

The digitized audio from the three RT's, intercom and "ALL" is fed into the serial inputs of the dual four-bit shift registers U34, U35, and U39. The data is clocked at 32 kHz and is available in four-bit parallel form at the shift register outputs to be multiplexed by U36 and U37. The three-bit address required to select one of five data lines is generated by counter U33. This counter is initially set to zero at the beginning of each frame by Latch so that the four bits of data from RT #1 (CVSD A in the schematic) is present at the output of the multiplexer and subsequently at the input of output shift register U11. The counter U33 is incremented on counts 107, 112, 117, and 122 so that the proper data is available at the inputs of U11 one full clock period before the LOD pulse.

The VIS Controller data output is taken from one of two shift registers, U2 or U11. Two sections of U13 and U17 form an AND/OR SELECT gate which is used to select between the two shift registers. Since the output of U9 pin 2 (OE1) directly indicates when frame sync data is being transmitted, this line is used to control the AND/OR SELECT circuit. Therefore, when OE1 is high, data is taken from U2 (frame sync data); and, when OE1 is low, data is taken from U11 (audio data).

6) Transmit PTT - Each of the eight users transmit PTT bits is loaded into U29 with the LID pulse and is steered to the proper RT with the latched destination address, MA1 and MA2, through multiplexer U28. One of three PTT circuits is shown in the schematic and consists of a gate, flip-flop, and a counter. If a user selects RT #1 and activates transmit PTT, a pulse will be generated at U25 pin 10 which is used to set the PTT line through flip-flop U9. Counter U18 is reset to zero each time any user activates the transmit PTT line and is incremented by LID for each user who does not request PTT for RT #1. In this way, all eight users must release their PTT requests before the output of U9 can be set low and turn off the PTT line. This is done to prevent unwanted toggling of the transmit PTT line to the RT.

i. User Station Schematic

Figure 4-6 is a schematic diagram of the presently breadboarded VIS user station. The following is a detailed discussion of the circuits described in the block diagram.

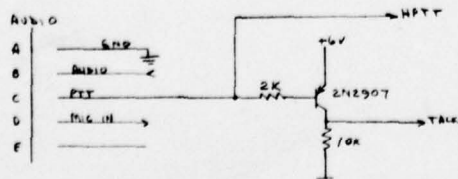
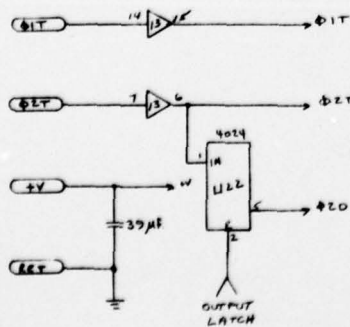
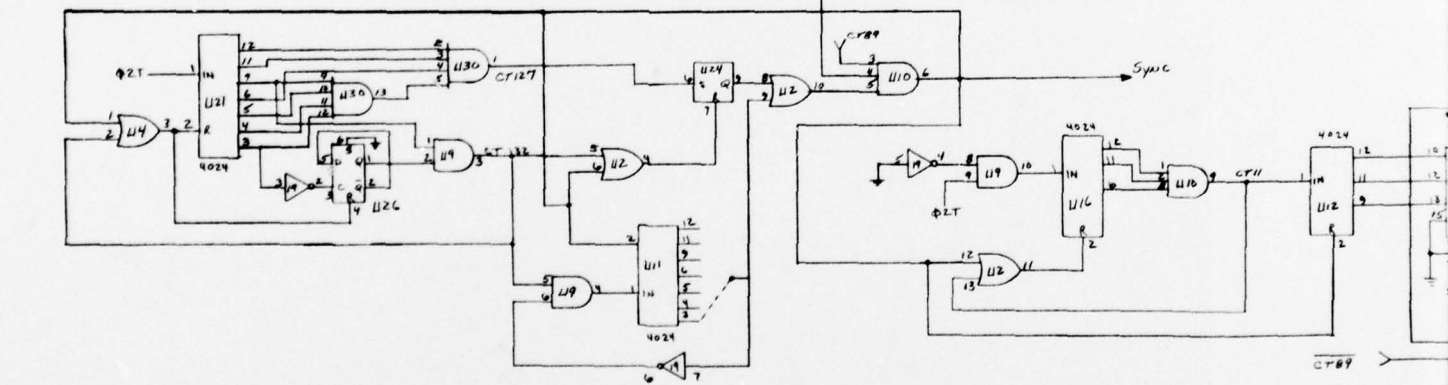
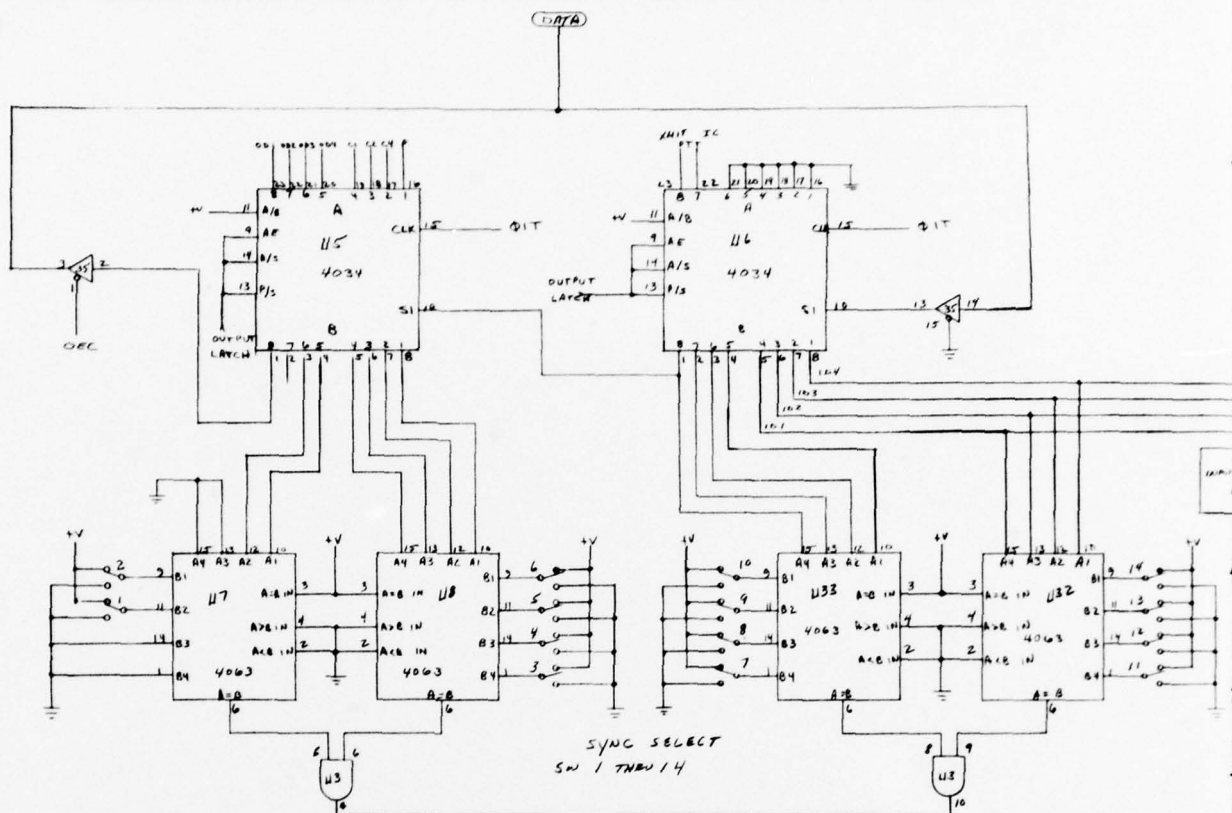
- 1) Clock - Both phases of the two-phase clock are received from the Controller and buffered by U13 before being used to clock the user circuitry. The $\phi 2$ clock is also divided down to create a properly phased 32 kHz clock for CVSD operation.
- 2) Data Shift Register - U5 and U6 create a serial in/parallel out; parallel in/serial out universal shift register. The serial data stream, buffered by U35, is clocked through this register and is converted to parallel form for further processing. The eleven bit (with guard) user data is loaded in parallel form into the shift register and clocked into the data stream at the proper time.
- 3) Sync Recognition and Recovery - The sync pattern search circuitry consists of U7, U8, U32, U33, and U3. U7, U8, U32, and U33 are each four-bit magnitude comparators whose A = B output goes high when the bit pattern at the A inputs precisely matches the predetermined B inputs. The switches at the B inputs are set to match the pattern created by the sync switches in the Controller. Magnitude comparators and switches were used in the breadboard only to facilitate sync pattern experimentation.

Each time the fifteen-bit sync pattern is seen on the data stream by the magnitude comparators, U3 pin 3 will go high for one bit time. This pulse when gated with the sync window circuitry is the user sync pulse.

The counter made up of U21 and U26 counts $\phi 2$ clocks with count 127 and 132 decoded at the output. At count 127, flip-flop U9 is set anticipating that a sync pulse will be recognized one clock later. If a sync pulse appears at U3 Pin 3 at this time, the system is synchronized and counter U21-U26 is reset to zero in order to count the next frame. In the event that a sync pulse does not occur on count 128, the circuitry continues to look for the sync pattern until count 132. If no sync pulse occurs in this five-bit window, missed sync counter U11 is incremented and counter U21-U26 is reset. This in effect delays the next sync search window by four bits. The sync search window is delayed up to 32 times if no sync pulse is detected, at which time, the sync circuitry is allowed to search the entire data stream with no window until a sync pattern is found. When a sync pulse is detected, the missed sync detector is reset to zero allowing the process to begin again. Once sync has been established, opening the search window only one bit early insures that the sync pattern, if present, will be detected at the proper time greatly reducing the probability of false synchronization. Even when the system is required to resort to searching the entire data stream, valid sync can be established in less than 50 ms.

IC Pinout Chart

IC	Pin	Type
U1, 2, 3, 25, 32, 33	16	8 4063
U2, 4	14	7 4071
U3, 9, 28	14	7 4081
U5, 6	24	12 4034
U10, 29	14	7 4073
U11, 12, 14, 15, 16, 17, 21, 22, 23	14	7 4024
U13	1	8 4050
U18	16	8 4061
U19, 26	1	8 4049
U20	14	7 40101
U21	16	8 4043
U26	14	7 4013
U27	16	8 MC1418
U30	14	7 4082
U31	14	7 4011
U34	16	8 4015
U35	16	8 40097



4) Output Data and Loading - The user station number is set into the circuit with the switches at the B inputs of the magnitude comparator U25. Counter U16 begins counting $\emptyset 2$ clocks after being reset by SYNC. This counter generates an output pulse every eleven clocks for the remainder of the frame period. These pulses are used to increment station counter U12 in order to create a three-bit code to correspond to the user station number which was preset as described above. The A = B output of magnitude comparator U25 will go high when the station counter output matches the station number switches. The positive going edge of this signal is converted to a pulse by U26 and U13. This pulse, called Output Latch, is used to load the eleven bit user data word into shift registers U5 and U6 at the proper time. The location of the Output Latch in time will be at Count 0, 11, 22, 33, 44, 55, 66, or 77 after SYNC depending on the user station number switch setting.

The four bits of digitized audio data are taken from the parallel output of the serial-to-parallel converter U34. The serial data stream comes directly from the CVSD encoder output and is clocked into the converter at a 32 kHz rate. The three-bit destination address, C1, C2, and C4, is taken directly from the user audio selector switches. Parity generator U20 outputs an even parity bit based on C1, C2, and C4. The transmit and intercom PTT bits are taken from the PTT switches, buffered and inverted by U36, and fed directly to U5 and U6. The guard bit is always low and is hardwired to ground.

5) Output Enable Control - The output enable control line is created from the A = B output of magnitude comparator U25. As discussed in the previous section, this line goes high when the user station time slot selected by the user station select switches is reached in the frame. This line then remains high for the eleven counts required to increment station counter U12 which then causes the A = B line to go low. This line is gated with the 89th count after SYNC to prevent enabling the output erroneously.

6) Input Data Selection and Loading - The user station must be capable of selecting one of the five last time slots in the frame depending on the user audio select switch. Since this data does not begin until the 89th counter after SYNC, count 89 from U15 is used to enable the input data selection circuitry. Counter U14 generates a pulse every five clocks which is used to increment counter U17 whose three bit output supplies time slot information to comparator U1. When the time slot information from U17 matches the audio source selected at the B input of U1, the A = B input of U1 will go high creating a single pulse, Input Latch, at U29 pin 9 which loads four bits of audio data from the data stream into U18. U18 is a parallel-to-serial converter/shift register clocked at 32 kHz to supply the digital audio data stream to the CVSD decoder input. The Input Latch pulse can be located at count 93, 98, 103, 108, 113 after SYNC, depending on the user audio select switches.

7) CVSD - The CVSD (U27) is a single chip audio encoder/decoder. With the EN/DEC pin low, the device takes the digital data stream at the digital input port and reconstructs the analog audio. With the EN/DEC line high, the converse occurs; analog data is converted to digital form.

g. System Operation

The TDMA intercom system just described has been breadboarded and tested. Both the Controller and User Station operate as described with the User Station breadboard operating properly in any one of the eight user assigned time slots. All information is properly handled between Controller and User with no degradation due to multiplexing.

h. System Tests

1) Audio Processing - The CVSD used in the TDMA intercom is the Motorola MC3418 which is optimized for 32 Kbps operation. Frequency response and total harmonic distortion measurements were made to determine a reference from which system degradation could be measured. The CVSD device has a sidetone output which is the result of encoding and decoding the audio at the analog input; measurements were made at this point. Figure 4-7a is the frequency response of the CVSD using an Allison Labs model 2AB low pass filter set for a 3 kHz cutoff at the sidetone output. Figure 4-7b is the total harmonic distortion also measured with the low pass filter at the sidetone output.

With the system operating normally, the user station was assigned the number one user time slot with the transmit PTT line keyed and the audio select switch set for RT #1. Audio response and distortion measurements were then made with the audio input at the user microphone terminals and the output taken at the RT #1 audio input terminals with the low pass filter again with a cutoff frequency of 3 kHz. This data is presented in Figures 4-8a and b.

An identical set of tests were conducted with the low pass filter cutoff frequency set at 6 kHz. The reference response and distortion data is in Figure 4-9, and the system data is in Figure 4-10. Although frequency response is within reason, harmonic distortion above 1 kHz is significantly higher than that obtained with a 3 kHz bandwidth. At this point, it would seem unwise to utilize a 6 kHz audio bandwidth in this system.

FIGURE 4-7a. CVSD FREQUENCY RESPONSE WITH 3 KHz LOW PASS FILTER

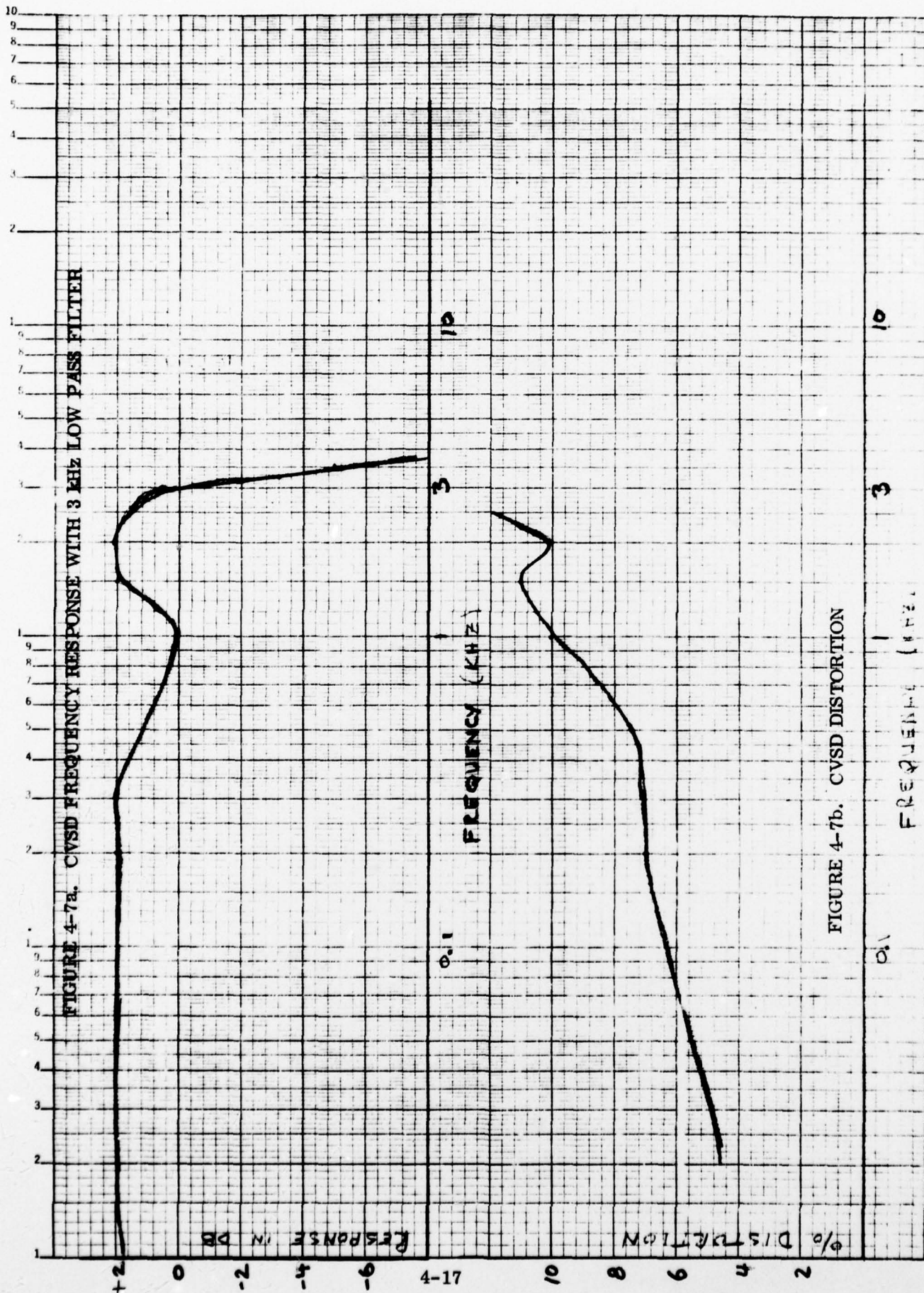


FIGURE 4-7b. CVSD DISTORTION

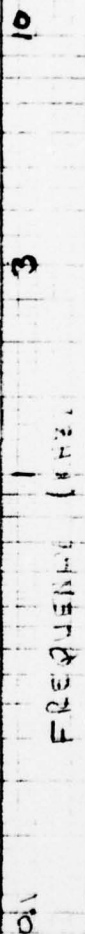


FIGURE 4-8a. VIS FREQUENCY RESPONSE WITH 3 KHz LOW PASS FILTER

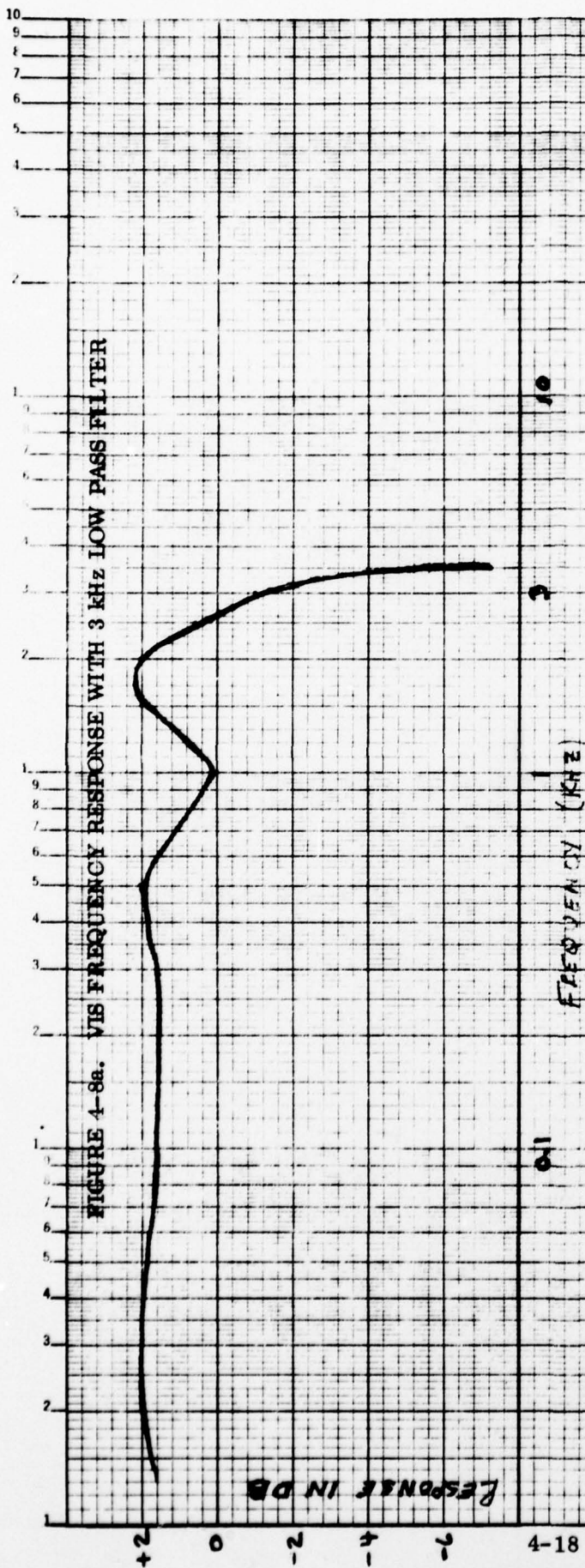
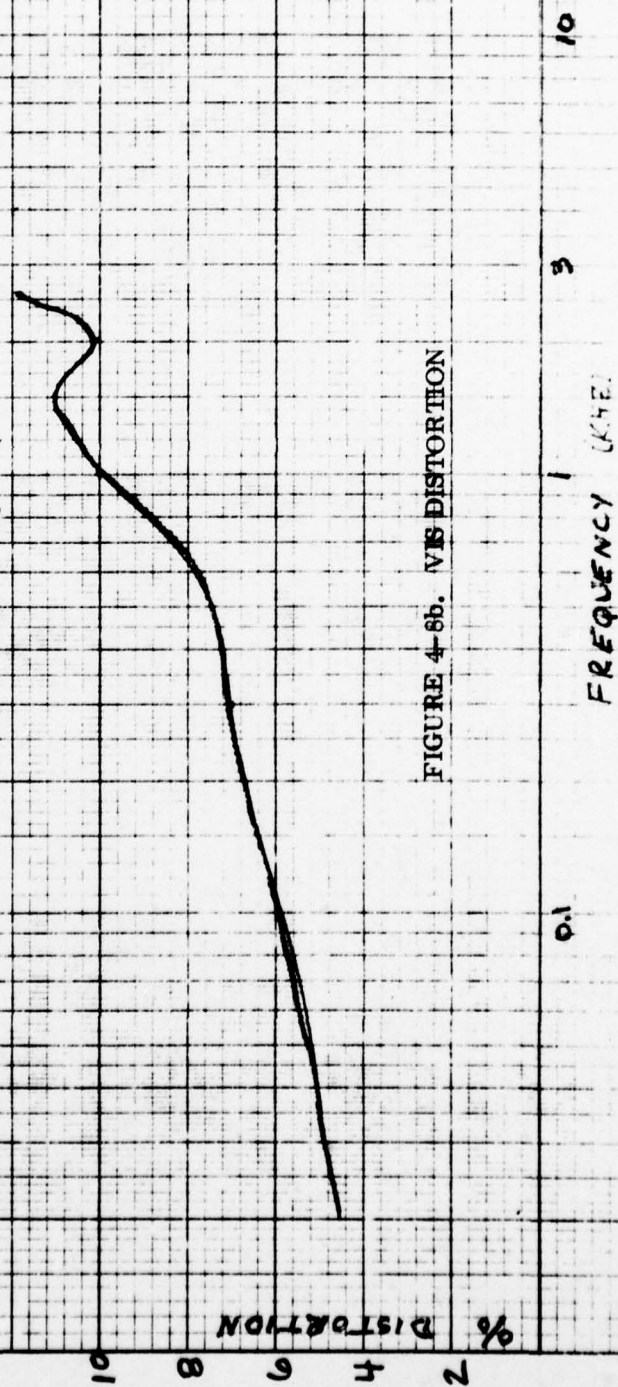


FIGURE 4-8b. VIS DISTORTION



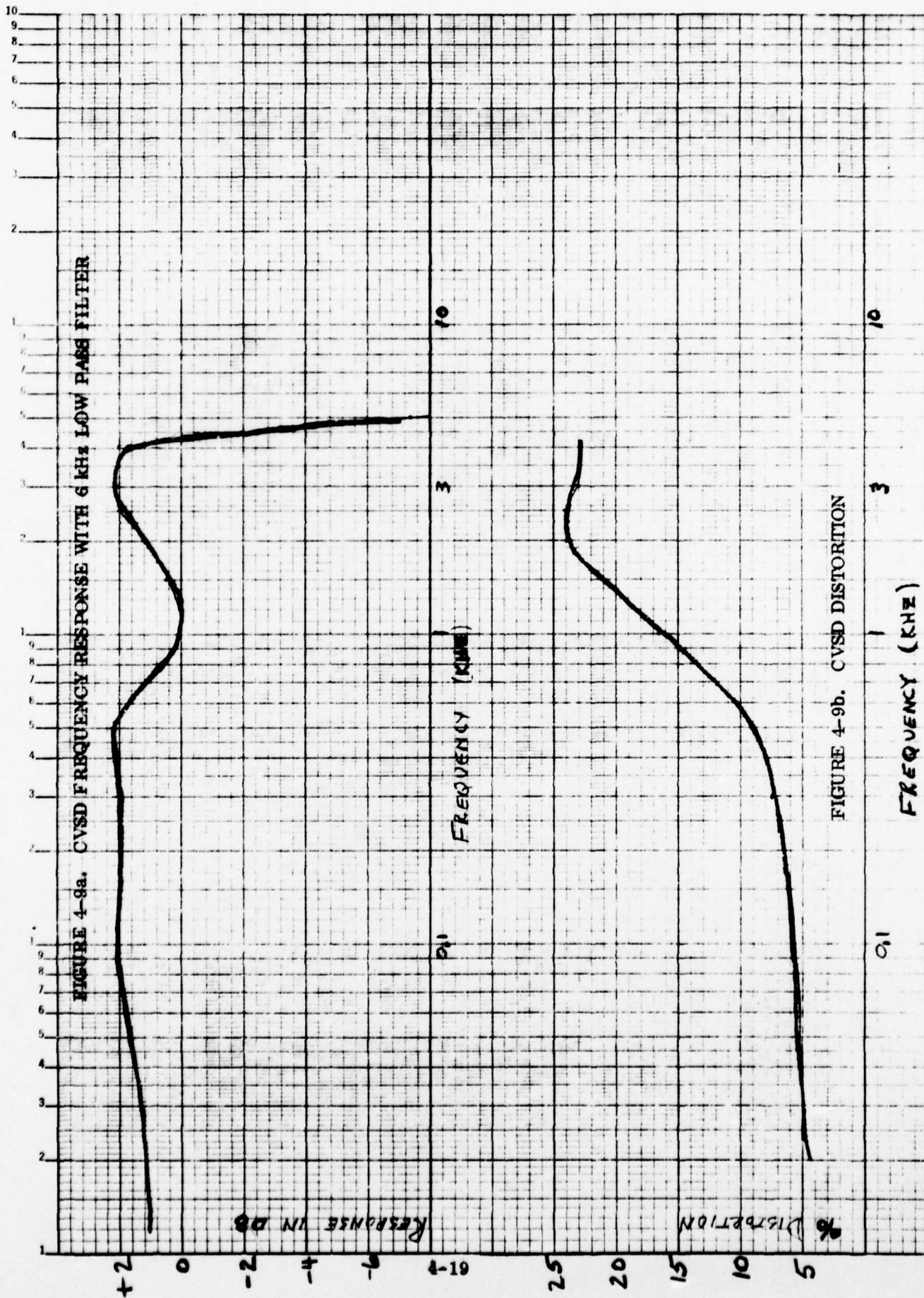


FIGURE 4-10a. VIB FREQUENCY RESPONSE WITH 6 KHZ LOW PASS FILTER

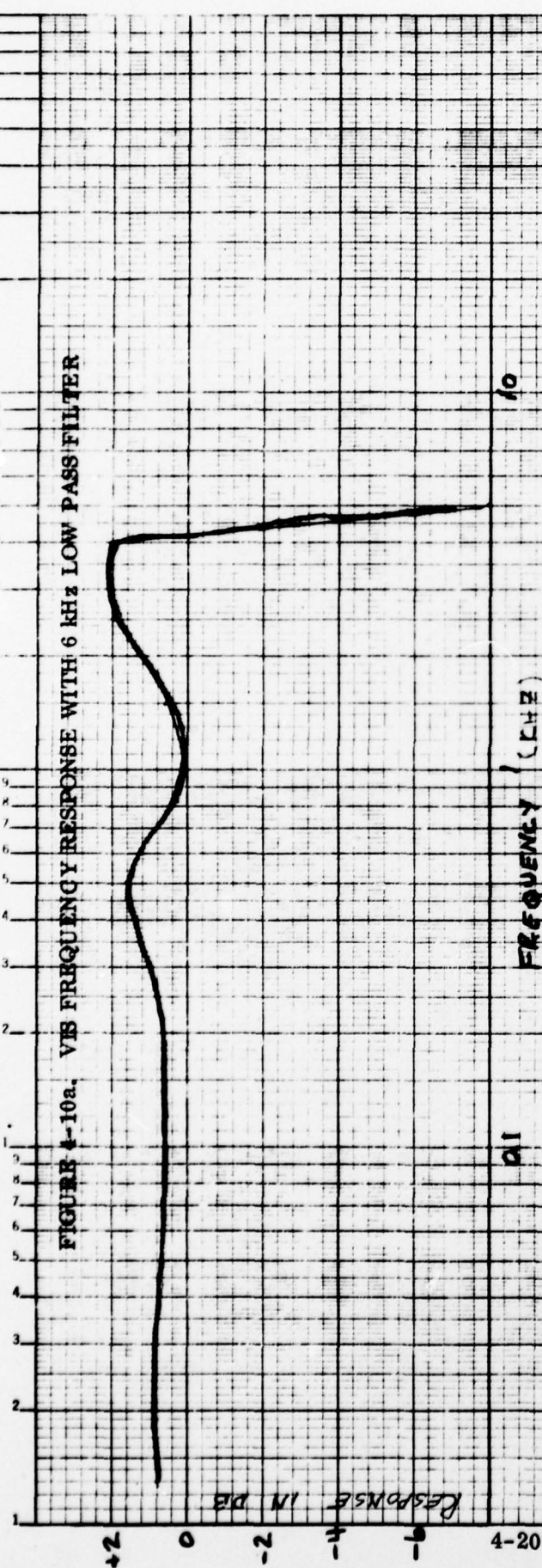
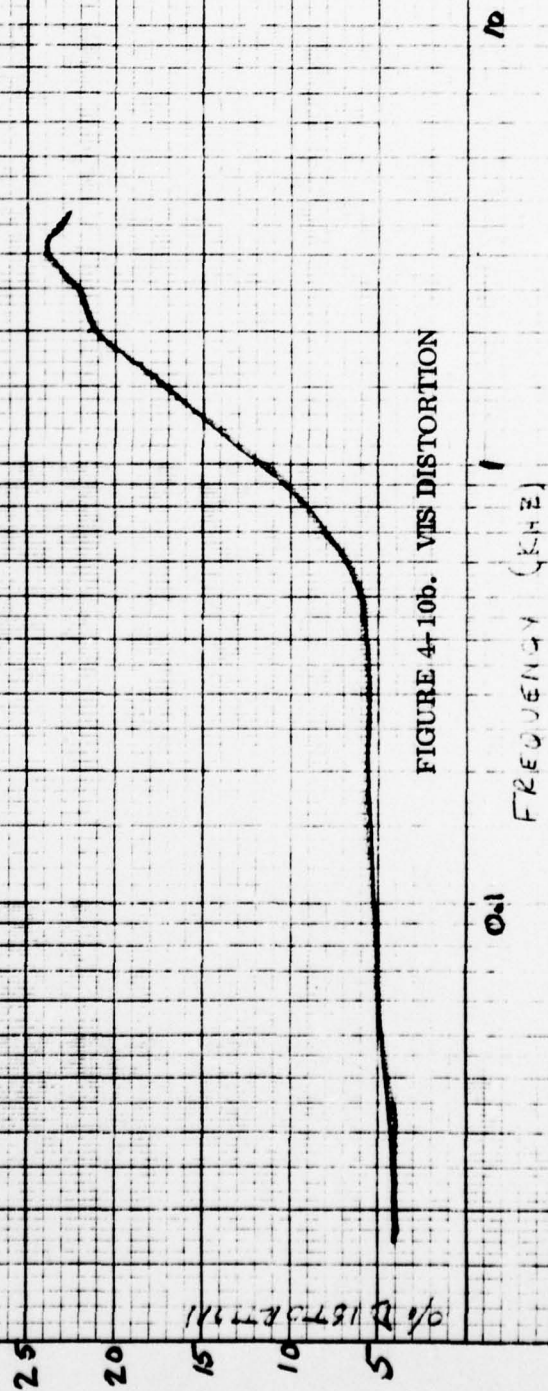


FIGURE 4-10b. VIB DISTORTION



It is not immediately obvious that the audio tests conducted are conclusive. In operating the system with actual voice information, it was found that the optimum CVSD gain and step size parameters do not correspond to the optimized settings used for steady state sine waves. This is true because the encoding/decoding algorithm is based on a complex rather than a simple waveform. Actual listening tests indicated that the system operating with a 3 kHz bandwidth sounds very good.

2) Synchronization Tests - Initial tests were conducted with only one user and the Controller putting data into the serial stream. The user station had no difficulty in establishing valid sync under these conditions since for every 125 μ S frame, only 50 μ S contained any data transitions. In order to simulate actual data for the remaining seven user time slots, a pseudo-random digital pattern was inserted into the data stream with the test circuit shown on the Controller schematic (see Figure 4-4). The gating arrangement shown in the test circuit allows the pseudo-random pattern to be inserted into the data stream only during user time slots two through eight. An HP 1645A Data Analyzer was used as a pseudo-random pattern generator with a pattern length of 1048575 bits and was clocked with the VIS 1.024 MHz clock. The data line as well as the two clock lines to the user station were randomly disconnected and connected to force missed sync and lost sync operation. In each case the user station regained system synchronization with no difficulty.

i. User Station Modification

In an actual intercom system, the user station would require an additional CVSD to provide a system sidetone to the operator during a PTT operation. The existing breadboard supplies the operator with his own sidetone; however, system intercom audio is blocked since the CVSD is acting as an encoder. The additional CVSD would be a dedicated decoder and would require an additional filter circuit. The control circuitry would not be affected.

j. Improvements

One possible area of improvement is in the system clock circuitry. The entire system could be redesigned to operate on a single phase clock to eliminate one additional cable. The single phase clock could then be modulo 2 added to the data output of the Controller. Each user station would then be required to have a high speed clock and sync circuitry to recover clock information from the Controller data. The intercom system would then require only one pair of wires to connect the entire system.

k. Plans for Next Quarter

Investigate data transmission problems over various lengths of pairs of wires.

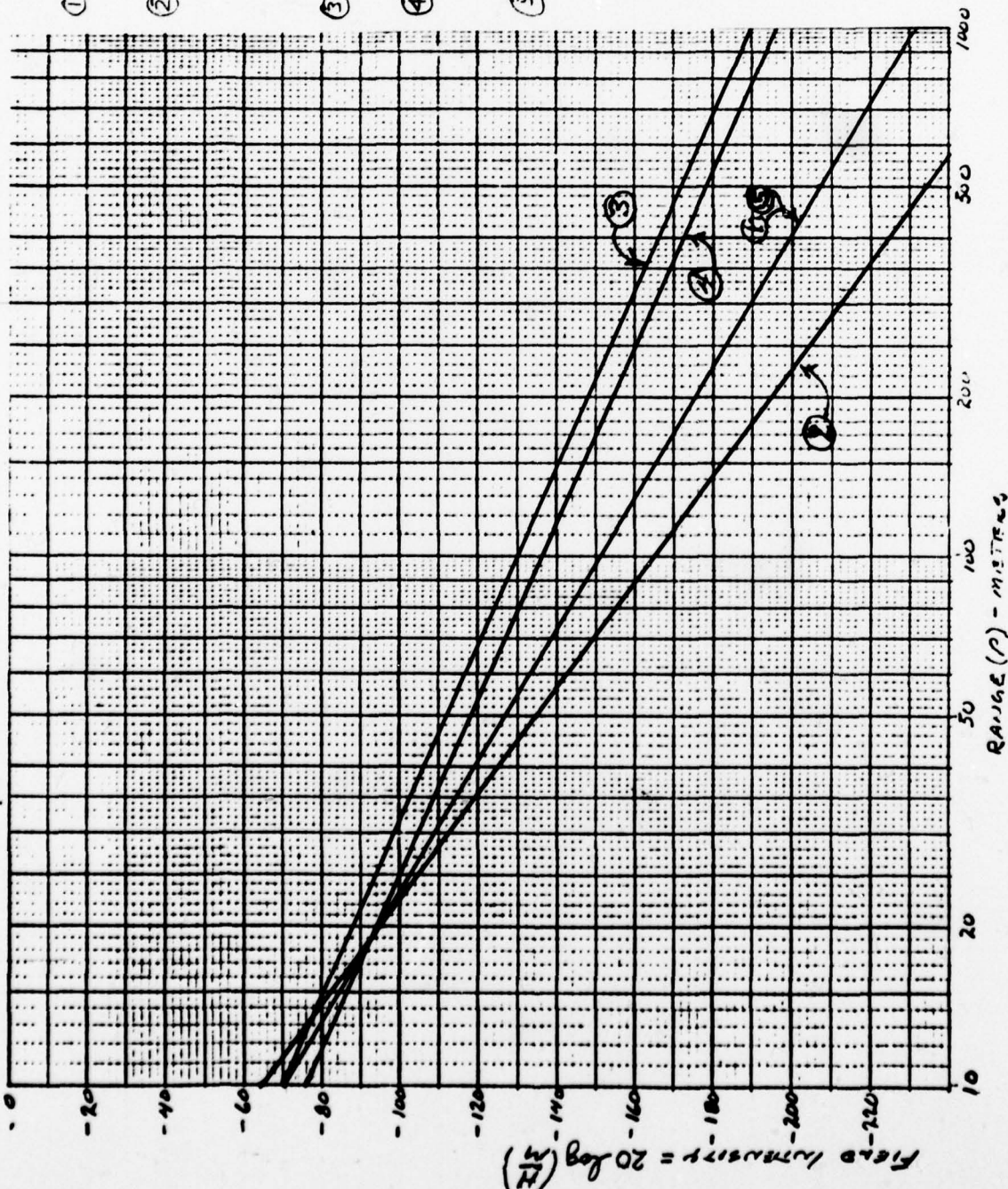
C. WIRELESS TECHNIQUES

1. Outside Station

At a program review meeting with the COTR, the following points were established relative to a wireless outside station:

- It is not acceptable to use a crypto system to provide security from enemy eavesdropping.
- Although a 50 meter range is desired, 15 meters would be acceptable if necessary due to reduced signal strength to avoid eavesdropping.
- The existing terminal on the rear of the tank should be used instead of requiring any new equipment mounting locations.

With the terminal location restricted to a point where the body of the vehicle blocks a line of sight to a significant percentage of the desired coverage area, microwave and infrared communications are ruled out. Eavesdropping would also be a problem with these systems. The only type of radiation which attenuates fast enough to afford reasonable security from eavesdropping is near field electromagnetic radiation from an antenna. Figure 4-11 shows the variation of signal strength for the magnetic fields radiated by vertical and horizontal magnetic dipoles. Due to its lack of directivity, the vertical dipole (horizontal loop antenna) is preferred. This antenna could also probably be built in a good form factor for vehicular mounting. If we consider curve 1 with the transmitting magnetic dipole just strong enough to provide a good signal-to-noise ratio at 15 meters, then at 50 meters, the signal would be reduced 42 dB which would produce a poor signal-to-noise ratio, but some signal might be detected. At 200 meters, the signal is reduced a total of 95 dB and at 400 meters, 115 dB. This should make it essentially impossible for an enemy to eavesdrop. Figure 4-12 shows the effect of varying the frequency and Figure 4-13 shows the effects of different types of ground. Further study during the next reporting period will be directed towards determining the required antenna sizes for both the vehicular and manpack stations and the transmit drive power requirements. If time permits, a breadboard system will be constructed.



VERTICAL MAGNETIC DIPOLE

① $\frac{H_p}{m} = \frac{3}{2\pi r^3} \mu$

② $\frac{H_z}{m} = -\frac{9}{2\pi r^3} \mu \sin^2 \theta$

HORIZONTAL MAGNETIC DIPOLE

③ $\frac{H_p}{m \sin \theta} = -\frac{1}{\pi r^3}$

④ $\frac{H_\phi}{m \cos \theta} = -\frac{1}{2\pi r^3}$

⑤ $\frac{H_z}{m \sin \theta} = \frac{3}{2\pi r^3} \mu \sin^2 \theta$

$\gamma = (-\omega^2 \mu \epsilon + j \omega \mu \sigma)^{1/2}$

NORMALIZING CONSTANT

$m = N I A$

(AMPS - TURNS - METERS²)

Range given in this figure is for $\epsilon_r = 30$, $\sigma = 0.031$, $\nu = 100$ kHz

FIGURE 4-11. AVERAGE LAND NORMALIZED H FIELD INTENSITY APPROXIMATIONS AT $f = 100$ kHz

DATA DRONE FIELD TYPE

VERTICAL MAGNETIC DRONE

① $\frac{H_p}{M} = -\frac{3}{2\pi \delta \rho_4}$

② HORIZONTAL MAGNETIC DRONE

⑤ $\frac{H_p}{M_{\text{max}}} = \frac{3}{2\pi \delta \rho_4}$

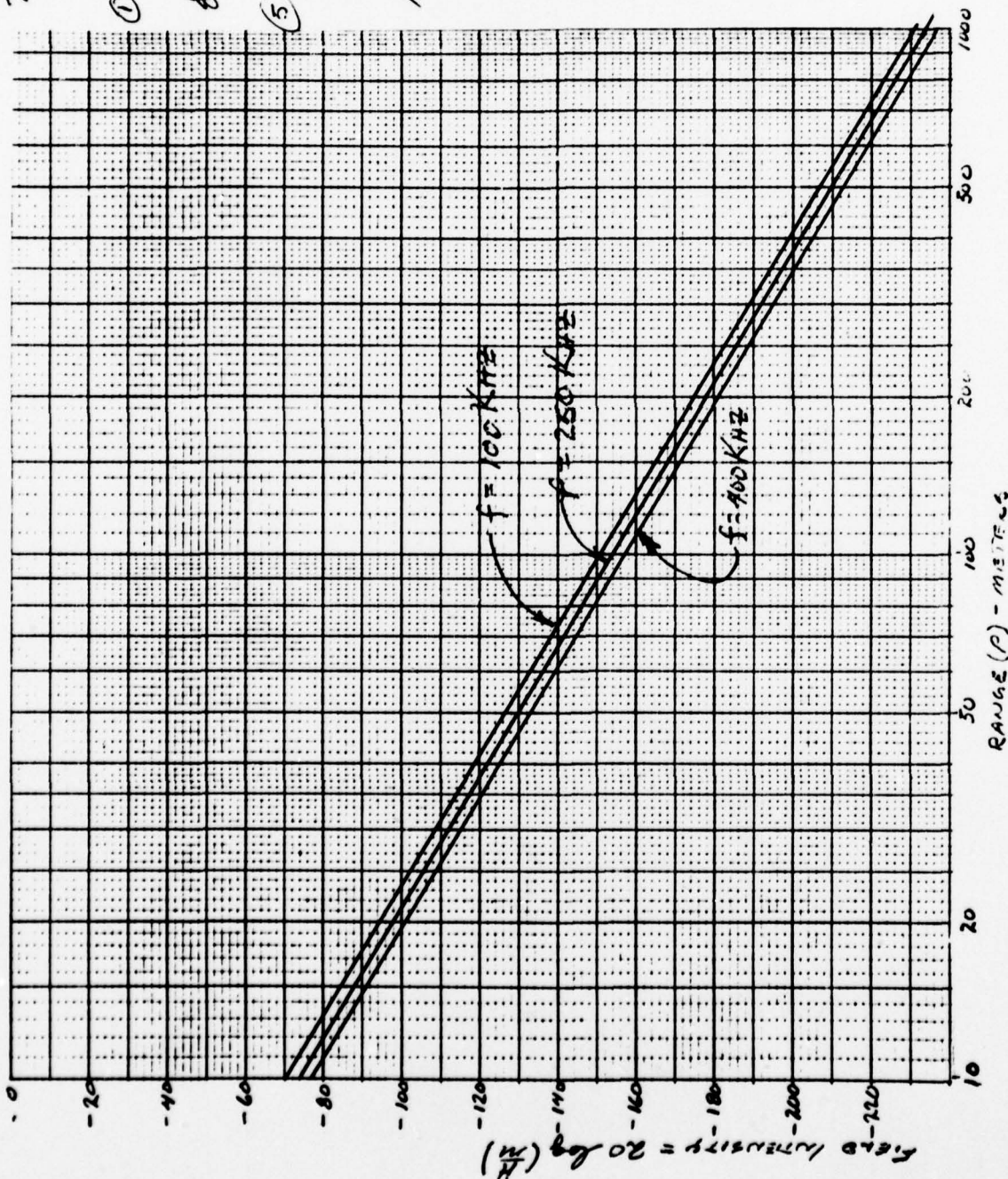
$\gamma = (-\omega \mu \epsilon + j \mu \sigma)^{1/2}$

NORMALIZED TO

MAGNETIC DRONE

$M = NIA$

(TURNS, AMPERES, METER²)



AVERAGE LAND ($\epsilon_r = 30, \sigma = 0.03 \text{ W/M}$)

RANGE GREATER THAN SKIN DEPTH, AND $\frac{H_p}{M}$ FIELD AND HND $\frac{H_p}{M_{\text{max}}}$ FIELD

FIGURE 4-12. NORMALIZED H-FIELD INTENSITY VS. FREQUENCY AND RANGE

DATA DERIVED FROM TYPE
VERTICAL MAGNETIC DIPOLE
 ① $\frac{H_p}{m} = -\frac{3}{2\pi r^3}$

② HORIZONTAL MAGNETIC DIPOLE
 ⑤ $\frac{H_p}{m \sin \theta} = \frac{3}{2\pi r^3 \sin^4 \theta}$
 $\gamma = (-\partial^2 u / \partial x^2 + \partial^2 u / \partial y^2)^{1/2}$

NORMALIZED TO
 MAGNETIC DIPOLE
 $M = NI A$

(TURNS AMPERES METER²)

GROUND CONDITIONS

δ_1 : SEA WATER

$\epsilon_r = 81, \sigma = 5.0 \frac{\text{V.M}}{\text{M}^2}$

δ_2 : FRESH WATER

$\epsilon_r = 81, \sigma = 0.005 \frac{\text{V.M}}{\text{M}^2}$

δ_3 : MARSH LAND

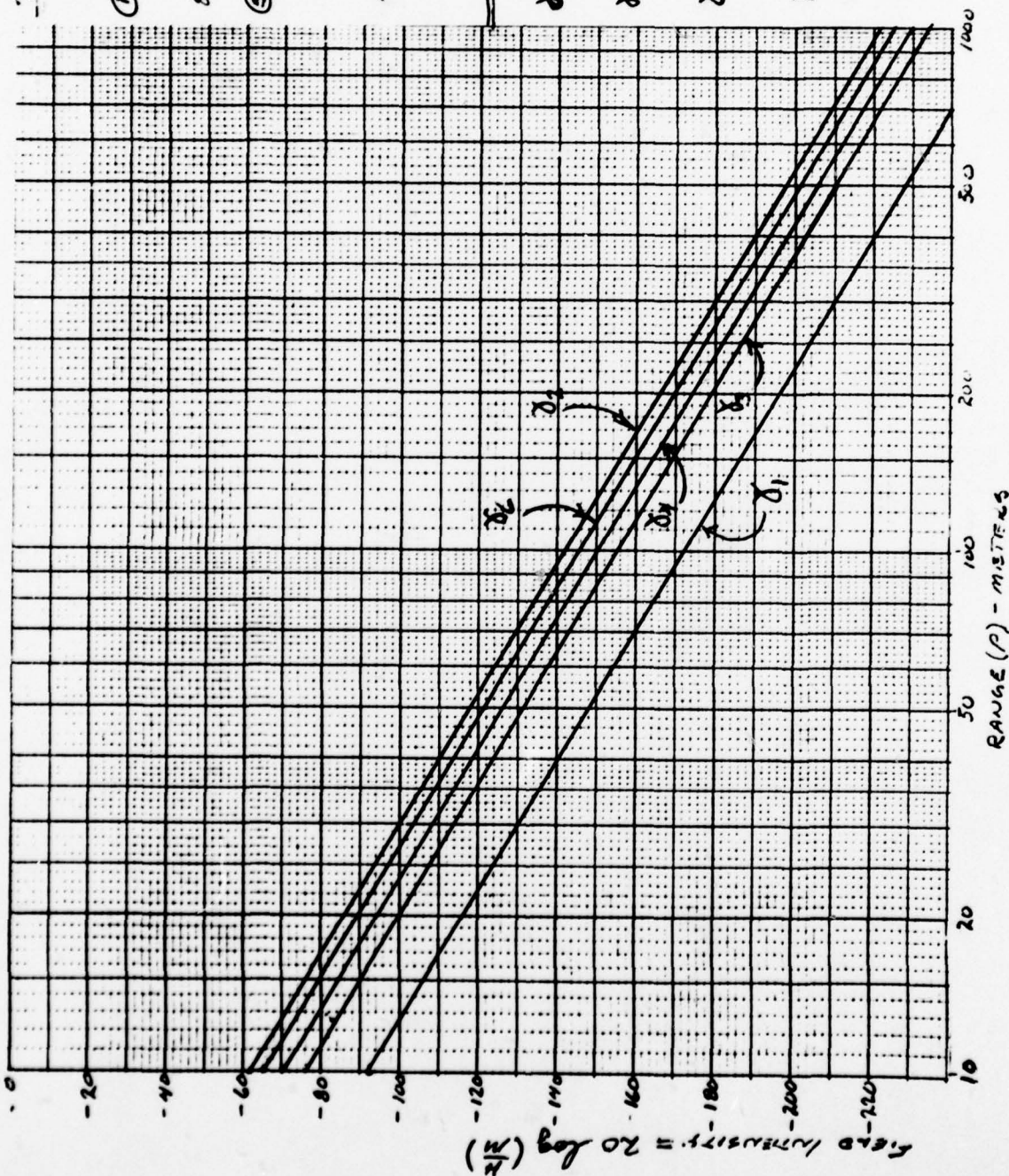
$\epsilon_r = 30, \sigma = 0.110 \frac{\text{V.M}}{\text{M}^2}$

δ_4 : AVERAGE LAND

$\epsilon_r = 30, \sigma = 0.030 \frac{\text{V.M}}{\text{M}^2}$

δ_5 : DESERT LAND

$\epsilon_r = 3, \sigma = 0.011 \frac{\text{V.M}}{\text{M}^2}$



Range (R) - METERS δ_1 SEA WATER δ_2 FRESH WATER δ_3 MARSH LAND δ_4 AVERAGE LAND δ_5 DESERT LAND

FIGURE 4-13. EFFECT OF GROUND CONDITIONS ON NORMALIZED H-FIELD INTENSITY

2. Inside Stations

a. Inductive Radiators

A breadboard system was constructed to investigate short range communications using the near field magnetic components of the electromagnetic radiation from a magnetic dipole. The circuitry was chosen for simplicity and convenience and does not necessarily represent the final design.

1) Transmitter - Figure 4-14 is a schematic of the transmitter. The microphone preamp delivers about 50 mV to the voltage controlled oscillator (VCO) input which results in 2.4 kHz peak deviation of the 50 kHz signal; 2.4 kHz was selected because it is the maximum deviation which can be used with a 6 kHz modulating frequency without exceeding the bandwidth of an amplitude modulated signal. The VCO output is amplified by an LM380 power amplifier. While the LM380 is intended to be an audio amplifier, its 100 kHz bandwidth is adequate for this application. The amplifier output drives a series resonant tuned circuit with a 400 turn coil as the antenna. About 3 VRMS is developed at the amplifier output.

2) Receiver - The receiver, shown in Figure 4-15, uses an antenna similar to the transmitting antenna but parallel resonant. A low noise FET preamp drives an active bandpass filter. Another amplifier increases the overall voltage gain to about 1000. A diode limiter protects the demodulator from overdrive. The FM signal is demodulated by a LM565 phase-locked loop (PLL) integrated circuit. The audio output of the PLL is filtered and amplified to drive a pair of headphones.

3) Performance - Preliminary measurements showed a signal plus noise distortion to noise plus distortion (SINAD) ratio of 28 dB at 1 meter separation between coils. Good quality voice was received with the receiving coil moved at least 2 meters from the transmitting coil. Most tests were performed with the axes of the coils approximately parallel (usually vertical). With the transmitting antenna axis vertical, the receiving antenna could be tilted at least 45° in any direction and moved above and below the height of the transmitting antenna with little effect on audio quality. It was possible to orient the antennas such that the signal drops down into the noise, but it doesn't seem to occur enough to warrant the use of crossed coils.

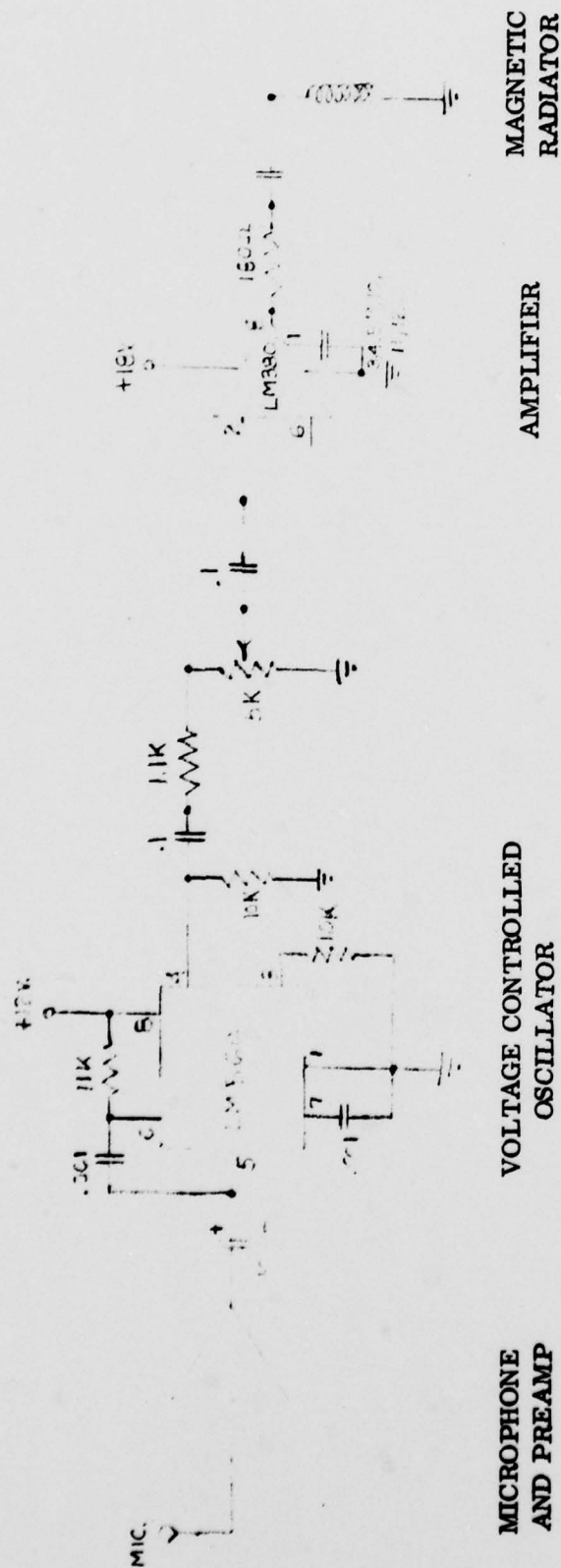


FIGURE 4-14. INDUCTIVE RADIATOR TRANSMITTER



FIGURE 4-15. INDUCTIVE RADIATOR RECEIVER

4) Future Plans - The breadboard circuitry will be rebuilt as a brassboard. This will eliminate some regeneration problems encountered in the receiver and allow both units to be packaged in a portable configuration. If the results of further lab testing are encouraging, field testing will be arranged. Although all work to date has been done at 50 kHz, the techniques will apply to other frequencies as well with minor changes to coil design and the use of higher frequency integrated circuits. At least two different frequencies must be used to provide two-way full duplex communication. It may also be necessary to provide a separate pair of frequencies for each station in a vehicle to insure each user's privacy, although this might also be accomplished by the normal physical separation between crewmembers. An analysis of signal bandwidth and adjacent channel rejection requirements indicate that 30 kHz spacing may be necessary, although careful allocation of channel assignments to take advantage of physical spacing might allow less frequency separation. With 30 kHz spacing, 8 users could be accommodated in the 50-500 kHz range, each user having unique transmit and receive frequencies.

b. Pulsed Systems

Two portable communicators were built to test pulses communications systems. They use a continuously variable slope delta (CVSD) modulator and demodulator to convert between voice and digital signals. They operate at 32 Kbps with a pulse width of 1.5 usec. They are housed in small aluminum boxes with rechargeable ni-cad batteries. One side of the box is left open so that different types of transmission systems can be attached for evaluation. To date, an infrared system has been built and a microwave system is being built. When both systems have been completed, they will be tried in whatever actual vehicles are available, probably at Fort Knox. A block diagram of the complete system is shown in Figure 4-16.

1) Infrared - Studies were conducted concerning signal-to-noise ratio versus range, communication link security, the availability of components, and atmospheric transmission properties. Pulse modulation of a source operating in the near infrared portion of the spectrum was chosen as the optimum system for the high background noise that is expected in vehicular operations.

In transmission, the output of the CVSD drives three infrared light emitting diodes (LED's) which emit radiation at a wavelength of 0.9 micron. One of these LED's, a Texas Instruments SL-1162, has a half beamwidth of 15° , the others have wider beamwidths. Each diode radiates approximately 5 mW of optical power.

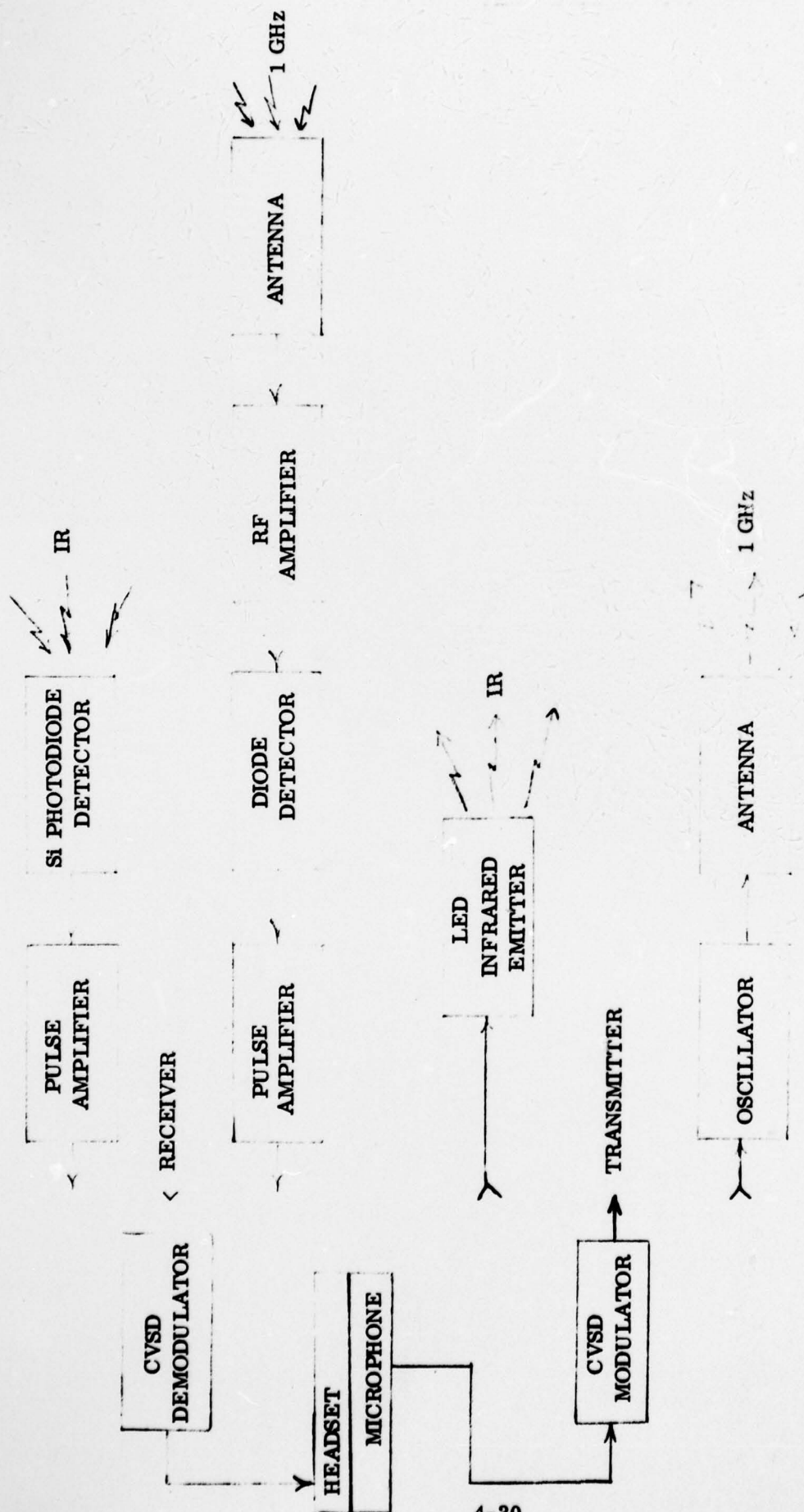


FIGURE 4-16. PULSED COMMUNICATION SYSTEMS

For reception, the detector is an RCA C30809 photodiode. The detected pulses are amplified and fed to the CVSD.

Lenses which narrow the transmitted beamwidth and receiver field of view can be attached for longer range communication. Calculations show that a signal-to-noise ratio (S/N) of 30 dB is expected using no lenses and with no obstructions inside the vehicle. This is about 15 dB greater S/N than necessary for successful communication. Dust and dirt on the emitter and detector diodes, as well as obstructions inside the vehicle, might degrade or disrupt communications in some cases. These effects will be evaluated in the field.

2) Microwave - A frequency of 1 GHz (wavelength of 0.3 meter) was chosen because it is low enough that efficient, inexpensive components are available, yet high enough that antennas, transmission lines, and reflection interference patterns are small.

The transmitter will consist of a Hewlett-Packard 35853E transistor oscillator with a matching network and antenna. The oscillator will deliver about +18 dBm to a 50 ohm load.

The receiver consists of an antenna, matching network, RF amplifier, detector, and low frequency amplifier. The RF amplifier has an HP HXTR-6104 transistor in the input stage and two succeeding stages using HP HXTR-6105 transistors. Its overall gain is about 38 dB. An HP 2787 diode is used for a detector. It will produce about 1 mV output for a -53 dBm input to the RF amplifier. Better performance could be had with a superheterodyne receiver, but the added cost is not felt to be necessary.

Both the transmitter and receiver will use flat plane high Q antennas consisting of a quarterwave length of 50 ohm transmission line on a .062 inch thick Teflon-fiberglass board to achieve an impedance match at 1 GHz. Separate antennas are used to avoid the need for duplexing or RT switching.

If this system proves to be successful, a sensitivity versus transmit power level trade-off study will be conducted to determine the optimum configuration.

D. BATTERIES

1. Introduction

To achieve the desired wireless audio accessories, batteries will be required to power circuitry attached to the crewmember since vehicle power cannot be wired to the crewmember for power. This section presents study results on batteries for this application. Since the battery field is continually changing, the results of this study are dated. Cincinnati Electronics will keep up with new developments and recommend changes where possible.

2. Primary vs. Secondary

Primary cells cannot be recharged; and, although they may cost 1/5 to 1/10 as much as a rechargeable cell, a rechargeable cell will outlast 100 to 1000 primary cells. Therefore, from an overall cost standpoint, the rechargeable cell will be less expensive than the primary cell. This is assuming a readily available charge source is present; the charger has a high MTBF and is not excessively expensive. Obviously, if the battery has to be transported to be recharged, the charger is expensive or maintenance costs are high for the charger; then, these expenses could outweigh the battery savings incurred with the use of rechargeable cells.

However, the above mentioned assumptions are valid for our application. The available charge source is the vehicular battery, and the charger described later in this section should not be expensive or unreliable. As a consequence, rechargeable cells are a reasonable choice from a cost savings standpoint for the VIS wireless audio accessories.

3. Types of Rechargeable Cells

Figure 4-17 shows presently available rechargeable cells and their corresponding energy densities. Since the battery pack has to be carried by the wireless crewmember, size and weight of the battery are important features. To reduce size and weight, high energy density is desired. However, the Silver-Zinc and Cadmium systems cannot be used because of their inability to operate at low temperatures. This and other disadvantages are shown in Figure 4-18. The next highest energy density system is the Nickel-Cadium. Nickel-Cadium batteries can be discharged at temperatures as low as -50°C. Nickel-Cadium batteries cannot be discharged at high current rates and lose considerable capacity at low temperatures. However, these disadvantages are also true for the Lead-Acid battery which is the next available battery system which can be discharged at -50°C temperatures. In addition, Lead-Acid batteries cannot be recharged as many times as Nickel-Cadium and require a complicated charger to prevent life reduction as a result of overcharge. Lead-Acid cells vent hydrogen gas during charge; and, although the quantity of gas release is small, it could accumulate inside a closed vehicle and present a safety hazard to crew personnel. For these reasons, Nickel-Cadium batteries have been chosen as a reasonable battery system for the VIS wireless application.

Typical discharge characteristics of secondary cells

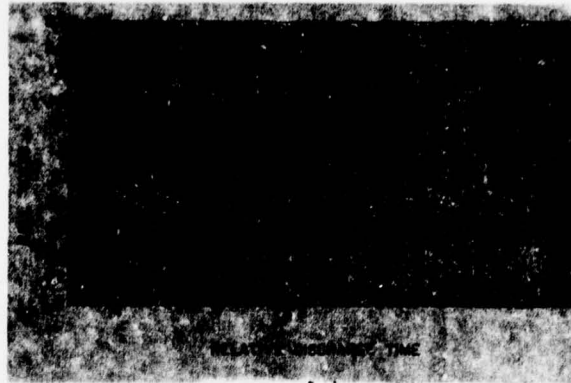


FIGURE 4-17a. TYPICAL DISCHARGE CHARACTERISTICS OF SECONDARY CELLS

Comparative energy densities of secondary cells

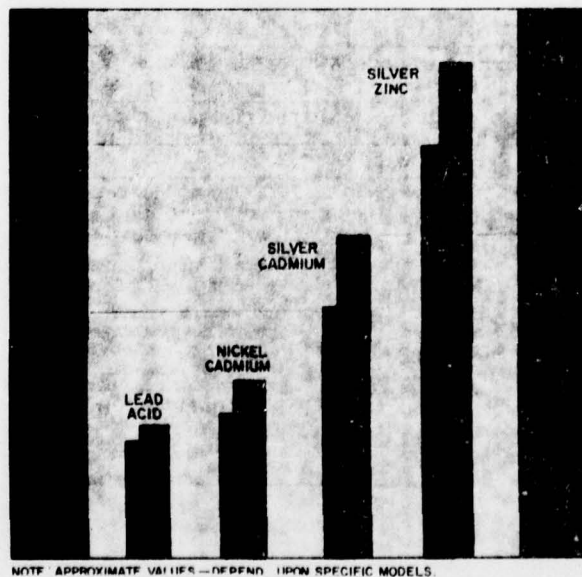


FIGURE 4-17b. COMPARATIVE ENERGY DENSITIES OF SECONDARY CELLS

SILVERCEL® AND SILCAD® CHARACTERISTICS

	SILVERCEL®	SILCAD®
Energy Output:		
Watt Hours/Pound	40-50	22-34
Watt Hours/Cu. In.	2.5-3.2	1.5-2.7
Open Circuit Voltage:	1.82-1.86	1.40-1.42
Voltage Under Load (Nominal):	1.5	1.1
Plateau Voltage Regulation:		
At Fixed Load and $\pm 10^{\circ}\text{F}$	2%	5%
Cycle Life:		
Dependent on Model and Usage Conditions. Typical Cycle Life to 80% of Nominal shown at Right.	LR Series — 80-100 Cycles	150-300 Cycles
	HR Series — 1 Hr Rate — 15-20 Cycles 30 Mn Rate — 10-15 Cycles 10 Mn Rate — 5-10 Cycles 6 Mn Rate — Single Cycle	
Operating Life:		
Wet Shelf Life — Normal (Varies w/ Temperature and State of Charge)	LR — 1 to 2 Years HR — 6 to 12 Months	2 to 3 Years
Dry Storage Life:	Up to 5 Years	Same
Operating Temp. Range:	+165°F to -10°F To -85°F w/Heaters Optimum Performance +125°F to +50°F	Same
Storage Temperature Range:	Wet +100°F to -55°F Dry +165°F to -85°F	Same
Operating Attitude:	In any position, except inverted. For optimum service, upright is recommended.	Same
Internal Resistance:	Very low. Varies with cell model design, temperature and discharge rate.	Same
Resistance to Mechanical Stress:	Excellent	Excellent
Both types have met the stringent requirements of Spec. MIL-E-527 2A and are currently used in missiles, rockets, torpedoes, and moon space applications. Extremely rugged, leakproof and spillproof, they can be packaged to meet the most severe requirements.		
Charging Time:	10 to 20 Hours	10 to 20 Hours
	Depending on Cell Design	Depending on Cell Design
Charge Completion:	Sharp voltage rise at 2.0 Volts/Cell	Sharp voltage rise at 1.55-1.60 Volts/Cell
Charge Retention:	Up to 65% retention of nominal capacity after 3 months charged stand at room temperature.	Same

FIGURE 4-18. SILVER CEL AND SILVERCAD CHARACTERISTICS

4. Battery Size and Voltage

The voltage output of a Nickel-Cadium cell is about 1.25 volts. To achieve voltages higher than this level, cells are connected in series. Generally, the more cells in series, the more expensive the battery for a given energy requirement. This relationship is shown in Figure 4-19. Each of the battery configurations shown in the table meet the 12 watt-hour energy requirement; however, the configuration with the least number of cells is the least expensive. Therefore, to minimize battery cost, it is desirable to have as few cells as possible.

On the other hand, in designing power supplies, Cincinnati Electronics experience has shown that voltages below about 5 volts cause an excessive increase in the inefficiency of a receiver/transmitter's power supply module due to higher currents and diode drops. Therefore, batteries with fewer than four cells were not considered.

The size of a battery is dependent on the energy requirement of the circuitry it drives. This energy requirement is expressed in watt-hours. To determine battery capacity, we divide the energy requirement by the battery voltage. This then would be the minimum battery capacity required. Unfortunately, battery capacity is not constant but is dependent on temperature as shown in Figure 4-20. This curve goes down to -30°C . Tests run here at Cincinnati Electronics indicate that at -50°C only 25% of the room temperature capacity is available. If we allow for battery aging, then five times the calculated capacity is a reasonable assumption to meet the energy requirement at low temperatures.

Nickel-Cadium cells are made which can be recharged at room temperature in four hours with a simple charger. Therefore, Cincinnati Electronics has assumed that a minimum of five hours before recharge is desirable. At this rate, a spare battery pack can be charged before the battery in use discharges. This allows almost continuous wireless operation except for time required to swap batteries. Also from a user standpoint, five hours minimum operation before swapping batteries seems reasonable. It should be noted that minimum time will occur at -50°C . Temperatures above this will give more time before recharge. At -30°C the minimum time will be ten hours and at the temperatures above -10°C the time will be eighteen hours.

Armed with these assumptions, battery configurations can be constructed to meet given circuitry power requirements. Figure 4-21 shows some battery packs as a function of the power required. These configurations minimize cost and size for the power levels shown, given that the assumptions are correct.

Batteries That Could Be Used for a 12 Watt-hour Energy Requirement

Battery Voltage	Rated Capacity, Ah	Rated Watt-hours	Number of Cells	Cell Size	Cell Model No.	Relative Battery Cost (%)
25	0.500	12.5	20	AA	GCF-500	230
20	0.600	12.0	16	A	GCK-600	190
12.5	1.0	12.5	10	C _s	GCR-1.0	120
8.75	1.5	13 $\frac{1}{4}$	7	C	GCT-1.5	110
6.25	2.0	12.5	5	$\frac{1}{2}$ D	GCW-2.0	105
3.75	3.5	13 $\frac{1}{4}$	3	D	GCW-3.5	100

FIGURE 4-19. BATTERIES THAT COULD BE USED FOR A 12 WATT-HOUR ENERGY REQUIREMENT

NICKEL - CADMIUM BATTERY CHARACTERISTICS

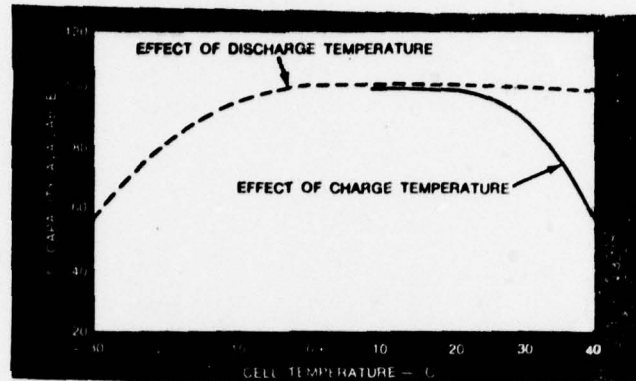


FIGURE 4-20a. EFFECT OF TEMPERATURE ON CAPACITY

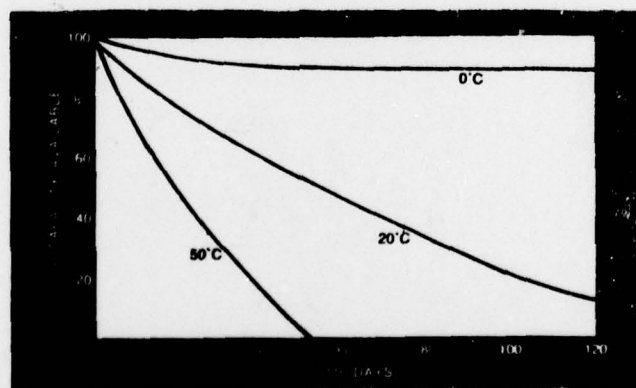


FIGURE 4-20b. EFFECT OF TEMPERATURE ON SELF-DISCHARGE

Average Power From Battery	Cell Size	Number of Cells	Battery Voltage	Minimum Battery Volume(in ³)	Minimum Battery Cost
250 mw	C _s	5	6.25	5.23	\$8.20
500 mw	C	5	6.25	8.10	\$11.05
750 mw	D	4	5.00	12.60	\$17.84
1.000 watt	D	5	6.25	15.75	\$22.30

- Assumptions:**
1. Five times capacity needed to offset loss of capacity at low temperature (-50°C) and as a result of battery aging.
 2. Five hours minimum operation desired before recharge.
 3. Battery voltages below 5 volts are undesired because of inefficiencies which will result in receiver/transmitter power supply circuits.

FIGURE 4-21. BATTERY VOLTAGE AND SIZE AS A FUNCTION OF POWER DRAWN FROM BATTERY

5. Battery Charger

Sealed cells are difficult to recharge at low temperatures because chemical activity is less and during overcharge excessive gas can be generated within the cell.

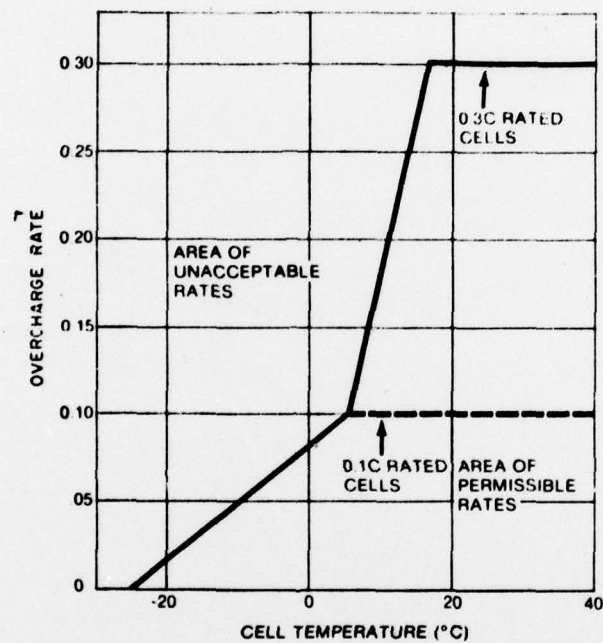
Figure 4-22 shows recommended overcharge rates as a function of temperature.

Since it is difficult to tell when a Nickel-Cadium cell is fully charged, stopping the overcharge is not possible. Therefore, the charger should be a box which encloses the charging battery packs and contains a heater to keep the inside of the box above 17°C.

Other than the low temperature problem, charging Nickel-Cadium cells is relatively simple. The cells are charged at a constant current for four hours; at which time, the rate of charge is reduced to a low level which prevents self-discharge as shown in Figure 4-20b.

A possible charger block diagram is shown in Figure 4-23b. Power for charging comes directly from the battery. The power required for charging is very small and should not noticeably discharge the vehicle battery with the engine not running. This feature insures charged batteries for the intercom. Power for the heater would only be on when the master switch was on. Unlike the battery charging operation, heaters require a significant amount of power and should not be on unless required. A temperature sensor would reduce charge rates if the heaters failed or were not turned on. A timer would reduce the charge rate after four hours.

Charge Characteristics



Permissible Overcharge Rates at Low Temperatures

FIGURE 4-22. PERMISSIBLE OVERCHARGE RATES AT LOW TEMPERATURES

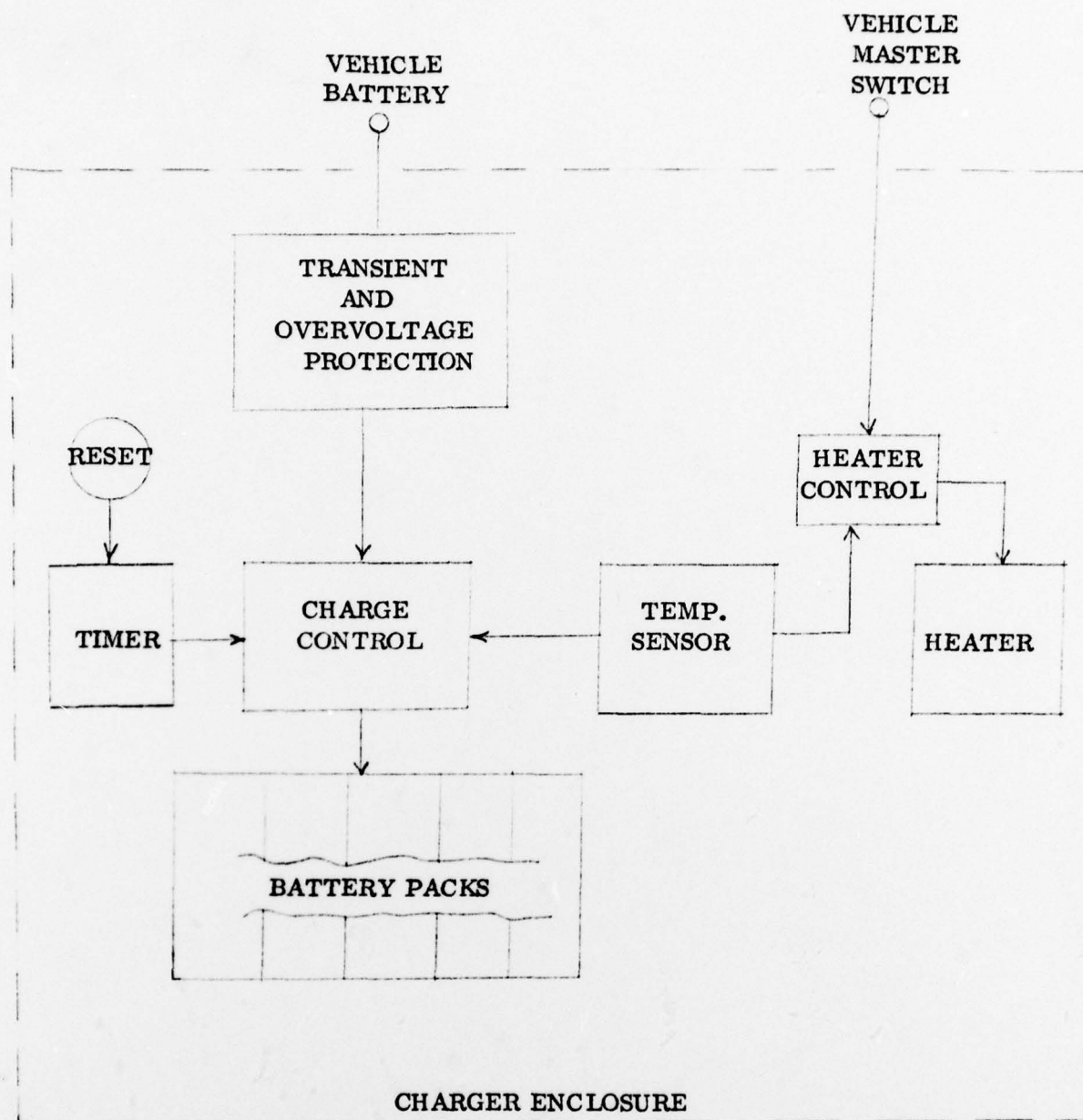


FIGURE 4-23. BATTERY CHARGER BLOCK DIAGRAM

SECTION V

LOGISTIC SUPPORT ANALYSIS

A. INTRODUCTION

An Optimum Repair Level Analysis (ORLA) utilizing the Generalized Electronic Maintenance Model (GEMM) was performed on both the Frequency Division Multiplexing (FDM) and Time Division Multiple Access (TDMA) approach. Since optimum wireless techniques had not been definitized at the time of the GEMM program run, parts lists for both systems reflect completely wired approaches. The results of the two approaches are summarized in the following paragraphs.

B. FDM APPROACH

The predicted Mean Time Between Failure (MTBF) of the FDM approach was 5022 hours. MIL-HDBK-217B, paragraph 3.0, "Parts Count Prediction", was used to determine the failure rate of each part. The Quality Level (uQ) criteria for parts were Class B for IC's, JAN'TX for semiconductors and level "S" for fixed resistors and capacitors.

The total life cycle cost, excluding Research and Development cost, for 50,000 units, was \$234.55 million. This cost is based on a maintenance philosophy of fault isolation to a box, module and piece part at the Direct Support level (GEMM Policy 16). This was the lowest Life Cycle Cost obtained from various combinations of maintenance policies.

C. TDMA APPROACH

The predicted MTBF of the TDMA approach was 4,351 hours. The same prediction method and quality levels used for the FDM were applied to the TDMA approach.

The total Life Cycle Cost, excluding Research and Development cost, for 50,000 units was \$389.12 million. This cost is based on the same maintenance philosophy (GEMM Policy 16) as the TDM and was the lowest cost of various combinations of maintenance policies.

D. CONCLUSIONS

Based on the two approaches pursued to date and from a completely wired standpoint, the FDM approach is the least complex, easier to maintain, has a lower Life Cycle Cost (savings of more than \$150 million), and is more reliable (5,022 hours MTBF vs. 4,351 hours MTBF). The FDM approach has the lowest Life Cycle Cost and would be the best approach based on total cost.

Details of the GEMM analysis can be obtained from the Draft Logistic Support Analysis Modeling (LSAM) Report, CLIN A004, dated May 1978.

E. NEXT QUARTER PLANS

Effort planned for the next quarter include:

- Perform GEMM analyses of the wireless approach.
- Perform sensitivity trade-off analyses of the final approach.
- Prepare the final submission of the LSAM report.

SECTION VI

PLANS FOR FINAL REPORT PERIOD

- A. Investigate data transmission over various lengths of wire for the TDMA system.
- B. Determine antenna and transmit power requirements for near field electromagnetic radiation for wireless outside station.
- C. Using portable breadboards of inductive, microwave and infrared wireless transceivers, Cincinnati Electronics will investigate potential problems in actual vehicles in coordination with the COTR and the Armor School at Fort Knox.
- D. Using Fort Knox results, select wireless system most suitable for vehicular environment.
- E. Generate necessary LSA data to allow GEMM program run on various feasible wireless system configurations.
- F. Using GEMM data and experience at Fort Knox, select optimum VIS system configuration.

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